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CHARACTERIZATION OF ELECTRICALLY ACTIVE
DEFECTS IN SI USING CCD IMAGE SENSORS.

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CHARACTERIZATION OF ELECTRICALLY ACTIVE
DEFECTS IN SI USING CCD IMAGE SENSORS
CONTRACT NO. N00173-76-C-0280

Errata

Page 11, paragraph 4, lines 3 and 4 should read:

lot. In addition, several slices from a control group were included to verify
the consistency of the processing from lot to lot.

Page 13, paragraph 1, line 7 should read:

topograph was actually a series of exposures with the photographic plate
placed as close as

Page 14, paragraph 1, line 4 should read:

defects were visible in x-ray topographs. This was a result of either the
small size

Page 18, paragraph 3, line 3 should read:

originated by prismatic punching. Certainly Figure 5(c) is consistent with

Page 21, paragraph 1, line 6 should read:

deposition and prior to the boron drive/thick oxide growth step; however, it

Page 44, paragraph 2, line 2 should read:

reaction $1/2\langle 101\rangle \rightarrow 1/6\langle 211\rangle + 1/6\langle 112\rangle$. The two partial dislocations are

Page 44, paragraph 3, lines 11 and 12 should read:

reported to occur when the dislocation is close to the screw (or 0° orienta-
tion).[11] The extrinsic stacking fault energy is deduced to be lower

<u>Page 101, paragraph 4, line 3 should read</u>:

appropriate in-contrast 220 reflection, and under conditions of exact Bragg reflection ($s \approx 0$).

<u>Page 119, paragraph 3, line 8 should read</u>:

of the Shockley partials is an easy process. The dislocation responsible

<u>Page 153, Figure C-1, should have the following note</u>:

*Indicates points at which in-process topographs were taken (Section IV).

<u>Page 154, paragraph 9, line 5 should read</u>:

if the carriers diffuse to the CCD wells.

FINAL TECHNICAL REPORT

CONTRACT NO. N00173-76-C-0280

30 July 1976 - 31 January 1978

Sponsored by
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Short Title of Work: Characterization of Electrically
Active Defects in Si Using CCD
Image Sensors

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TECHNICAL REPORT SUMMARY

The purpose of the work ~~under Contract No. N00173-76-C-0080~~ has been to characterize electrically active defects in silicon using a CCD area imager as a test structure. CCD imagers have been fabricated on a variety of substrate materials and operated to determine the location and density of dark current producing defects; the defects have been characterized by x-ray topography and by conventional and scanning transmission electron microscopy.

Four classes of defects with five specific origins have been found to be dark current sources:

(1) Dislocations from device stresses, from process stresses, and from the unfaulting of stacking faults.

(2) Stacking faults nucleated from frontside damage.

(3) A defect located at the Si/SiO_2 interface.

(4) A defect of atomic dimensions that causes banding in the dark current pattern.

No evidence of precipitation was found on any dark current producing defect. The electrical activity of dislocations is consistent with a model in which undissociated perfect dislocations in the depletion region are dark current sources, while dissociated dislocations (split into two Shockley partial dislocations) are not electrically active.

Both backside mechanical damage by glass bead sandblasting and Impact Sound Stressing (ISS) have been found to be only slightly beneficial, at best, reducing the number and intensity of dark current spikes, but not eliminating them. Bulk swirl precipitation of oxygen underneath CCD imagers has been found to be capable of very effective gettering, with some imagers found to be defect-free.

The unfaulting of stacking faults has been studied, and an impurity, probably oxygen, has been found to be adsorbed onto stacking faults. Under certain circumstances, this impurity precipitates during the unfaulting process, gettering copper. Subsurface nucleation of stacking faults has been observed and determined to be nucleated by oxygen and copper. It appears that this is the source of stacking faults in CCD imagers.

Orientation of the device channel stops in $\langle 100 \rangle$ directions has been used successfully to suppress device stress generated dislocations.

It is believed that the best material for CCD imagers is Czochralski-grown silicon which produces bulk precipitation of oxygen. Backside gettering may be used generally, but will not improve the performance if bulk precipitation is present.

Additional research is necessary to specify the material parameters and treatment which produce bulk precipitation. While a high oxygen content is necessary, it has not been found to be sufficient. Other areas of recommended investigation include the development of an incoming quality control screen for low defect material, the determination of the effectiveness of other backside gettering techniques, and the development of low-defect processes which minimize thermal oxidations.

SECTION I

INTRODUCTION

The purpose of the work under Contract No. N00173-76-C-0280 has been to characterize electrically active defects in silicon using a charge coupled device imager as a test structure. Since the CCD imager is essentially an array of MOS capacitors, each approximately $645\,\mu m^2$ ($1.0\,mil^2$) in area, it provides an excellent way to pinpoint crystalline defects whose electrical activity produces leakage current in the depletion layer of an MOS device. With the device that has been used in these studies, imagers on a 7.6 cm (3 inch) slice constitute in excess of 3,000,000 MOS capacitors. The CCD structure provides a simple means of reading these capacitors and presenting the large quantity of information.

Three benefits accrue from using the small MOS capacitors of the CCD imager rather than a larger MOS test structure:

(1) The precise location of an electrically active defect is determined. This enables a search of a specific location by other means to determine the cause of electrical activity.

(2) Information on the density of defects in a specific area is obtained. This enables a search to be made of this area for defects present in that density.

(3) The CCD imager sees a full processing cycle, as compared to a single oxidation for most MOS test capacitors. This means that the defects produced will be typical of those that cause problems in real devices.

For structural characterization of the defects, diffraction methods are well suited. X-ray topography is capable of resolution to $\sim 1\ \mu m$, but generally is capable of imaging defects no smaller than 5 μm. Where defects are imaged, however, it is possible to make one-to-one correlations of defects and electrical activity. Our experience has shown that the two classes of

defects that are imaged in devices are dislocations longer than ~ 5 µm and stacking fault clusters. In addition, transmission x-ray topography is capable of imaging defects throughout the bulk of the wafer and therefore is useful in understanding the operation of "gettering" mechanisms.

Higher resolution requires the use of transmission electron microscopy. Here the sample is thinned to ~ 1 µm and observed in transmission. Using weak beam techniques, precipitate particles as small as 15 Å have been imaged on dislocations. The inherent disadvantage of transmission electron microscopy is that only a portion of the depletion region can be examined, i.e., a 1 µm thickness of the 5 µm deep depletion region.

For chemical characterization, the x-ray analytical capabilities of a scanning transmission electron microscope are ideal. Using this instrument, it has been possible to detect copper in precipitate particles ~ 100 Å in diameter. It is estimated that these particles contain $\leqslant 10^5$ atoms of copper.

A. Organization of Research and Report

The organization of this report largely follows the execution of the research program. To assist those unfamiliar with the defect nomenclature, a brief summary is presented in Appendix A. At the beginning of the program, material for devices was obtained and processing initiated. The operation of the device chosen for this program and an outline of the front-end process are contained in Appendixes B and C, respectively. While we were awaiting processed devices, slices containing devices were made available for initial evaluation. These preliminary observations are reported in Section II. Also during this period, improved x-ray topography techniques and sample preparation techniques for electron microscopy were considered. These are reported in Appendixes D and E. The bulk of the work characterizing defects in imagers is reported in Section III. This section contains results on a variety of materials, both with and without backside mechanical damage.

Simultaneously with this main thrust, two additional series of experiments were conducted. The first of these consisted of a study of the evolution of defects during processing. In this experiment, a group of slices was processed, with transmission x-ray topographs taken of each wafer after each high temperature step. The results of these investigations are reported in Section IV. The second set of experiments was conducted to understand the evolution of stacking faults during the course of processing. The results of these experiments, which provide a significantly improved understanding of stacking faults, dislocations, and the effect of trace amounts of copper in silicon, are presented in Section V. This information has proved vital in understanding the causes of defects in CCD imagers.

Section VI presents a discussion of all of the experimental results, addressing three important questions: (1) What are the dark current producing defects in CCD imagers? (2) Why are they electrically active? and (3) What are their origins? In this section, models for electrical activity and scenarios for their evolution are presented.

The final section of this report, VII, makes specific recommendations for future work and for possible ways of producing CCD imagers and/or VLSI devices with few or no dark current defects.

B. Summary of Significant Findings

(1) Four classes of defects with five specific origins have been found to be dark current sources:

- Dislocations from device stress, from process stresses, and from the unfaulting of stacking faults whose origin is sub-surface bulk nucleation.
- Stacking faults nucleated from frontside damage.
- A defect located in the Si/SiO_2 interface.
- A defect of atomic dimensions that causes dark current banding.

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(2) No evidence of precipitation and no detectable impurities have been found on any defects in CCD imagers.

(3) Electrical activity is attributed to the presence of undissociated perfect dislocations and Frank partial dislocations in the depletion region of the device. Dark current spikes are visible when there is sufficient length of these defects in the depletion region.

(4) Only the interface defect is "gettered" by backside mechanical damage produced by glass bead sandblasting. The total dark current, however, is significantly reduced.

(5) Impact Sound Stressing (ISS) has been found to be no more effective than backside damage by glass bead sandblasting in eliminating dark current spikes.

(6) Imagers located over regions of a slice containing bulk swirl precipitation of oxygen contain significantly fewer dark current spikes than devices over regions containing no bulk swirl precipitation. Frequently, these devices are defect-free.

(7) The atomistic defect causing dark current banding responds to short-range gettering(< 50 μm).

(8) The unfaulting of stacking faults has been studied, and the pertinent dislocation reactions have been deduced.

(9) Stacking faults in silicon have been found to contain a large quantity of adsorbed impurity ($> 10^{14}$ atoms/cm^2 of stacking fault). It is deduced that this is primarily oxygen.

(10) Evidence that copper is adsorbed to stacking faults has been found in experiments independent of imager processing.

(11) Evidence has been found that the subsurface nucleation of stacking faults is caused by trace amounts of copper.

SECTION II
PRELIMINARY OBSERVATIONS

A. Introduction

To determine the effect of material variability on the dark current performance of CCD imagers, two series of experiments were undertaken. In the first series, standard starting materials of various types were used, devices fabricated, and total dark currents compared. In the second set of experiments, the effect of backside mechanical damage on total dark currents was examined.

B. Results

Forty-five wafers were processed in the first lot, including 15 Varian-pulled Czochralski wafers, 15 wafers from a standard TI rf-heated Czochralski puller, and 15 Wacker float-zone slices. Devices that passed multiprobe tests were mounted on dual-in-line ceramic (CDIP) headers and characterized for image quality and total dark current. Results of the dark current measurements are shown in Table 1. Conversion of total dark current to nA/cm^2 requires that figures in the table be multiplied by 1.85. Figure 1 shows placement of bars on a 7.62 cm (3 inch) wafer by device number.

Results of this experiment were surprisingly conclusive. Since all wafers were subjected to each processing step together and were randomly mixed in diffusion boats, differences among wafers can be considered to be largely a result of starting material. Examining dark current levels for any given wafer number reveals a statistically significant grouping. Although the number of devices tested is too small to be certain, it appears that a given starting wafer will tend to yield devices with dark current levels of the same order of magnitude if process variables are held constant.

<u>Table 1</u>
<u>Dark Current Measurements – Lot #1</u>

<u>Wafer #</u>	<u>Device #</u>	<u>Material</u>	<u>Total Dark Current (nA)</u>
RF-9	27	RF-Heated Czochralski	4.3
RF-11	9	↓	6.1
RF-11	26		5.0
RF-15	14		63.0
RF-15	20		138.0
RF-15	33	RF-Heated Czochralski	89.5
W-10	16	Wacker float-zone	153.7
W-10	22	↓	29.8
W-11	5		14,600
W-11	9		250,000
W-11	23		350,000
W-12	17		150.0
W-13	21		34.7
W-13	22	Wacker float-zone	83.0
V-3	4	Varian Czochralski	56.3
V-3	6	↓	55.8
V-3	33		71.8
V-4	10		19.2
V-4	28		5.9
V-4	34		7.0
V-13	21		5.2
V-13	27		5.1
V-13	29		13.3
V-14	27		4.4
V-15	4		815
V-15	5		280
V-15	26		168
V-15	32		619
V-16	21		5.8
V-16	22		8.5
V-16	27	Varian Czochralski	4.4
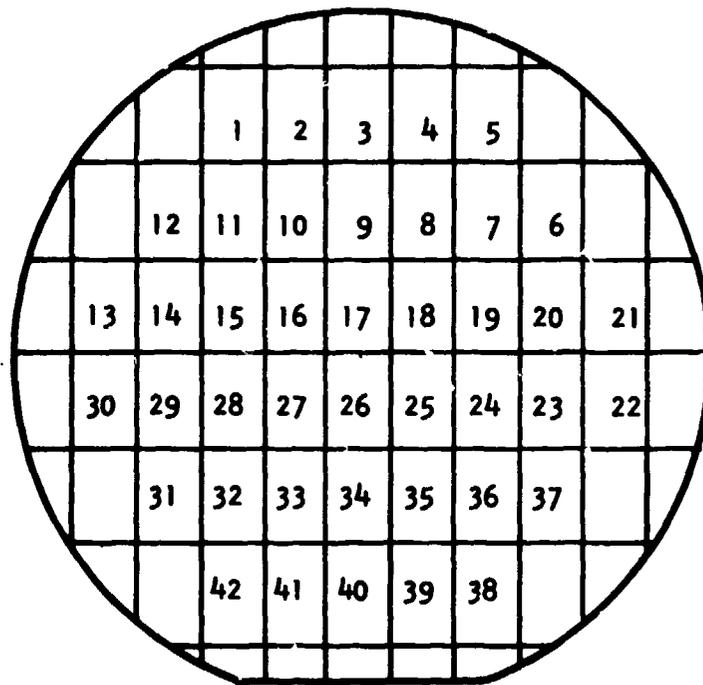
Figure 1   Device Number Positions on 7.6 cm Slices

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A second result is also apparent from Table 1. The Wacker float-zone material yields a significantly higher level of dark current than either of the two types of Czochralski material. Comparison of the lowest dark current devices from each of the three groups gives 4.3 nA for rf-heated, 34.7 for Wacker float-zone, and 4.4 for Varian Czochralski. Corresponding average values are 51.0 nA, 76,881 nA, and 126.2 nA, respectively. Elimination of the worst Wacker wafer reduced that value to 90.24 nA, while the rf-pulled group would become 5.1 and the Varian, 20.2 nA.

Device dark current shows no clearly detectable trend with placement on the wafer, but the number of devices in this test is too small to attach meaning to this observation. Since devices from each of the three material groups appear to be randomly placed on the wafers, there is no reason to believe that placement affected the results seen in comparing the three groups.

Comparison of the float-zone results with Czochralski Si suggests that the reduced oxygen content achieved with float-zone techniques may not be the most important variable for controlling dark current. A possible explanation relates to the observation that the Wacker slices were heavily stress-relieved on the back surfaces. The two types of Czochralski material retained substantial backside damage from final grinding and therefore may have exhibited backside damage gettering.

A second experiment was conducted using three groups of silicon: (1) Varian Czochralski wafers with sandblasted back surfaces, (2) Shin-Etsu wafers with standard stress-relieved back surfaces, and (3) Varian Czochralski wafers with lightly stress-relieved back surfaces. Unfortunately, there were not enough good devices from this test to draw absolute conclusions, but there are some strong indications of material effects. Results are summarized in Table 2. The small number of Varian Czochralski wafers with sandblasted backsides

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Table 2
Dark Current Measurements -- Lot #2

Wafer #	Device #	Material	Total Dark Current (nA)
V-6	9	Varian Czochralski - sandblasted	16
V-6	14	↓	23
V-6	34	Varian Czochralski - sandblasted	10
SE-7	2	Shin-Etsu	172
SE-7	4		34
SE-7	6		32
SE-7	15		363
SE-7	25		143
SE-7	27		19
SE-7	32		20
SE-7	38		22
SE-7	39	Shin-Etsu	25
V-10	28	Varian Czochralski - standard backside	232
V-37	22	↓	28
V-37	30		31
V-37	33	Varian Czochralski - standard backside	41

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do appear to show lower dark current levels than the same Varian slices without the backside damage. The Shin-Etsu silicon does not show significant improvement over standard Varian Czochralski Si, but is not significantly worse, either. Here again, the "near-polish" on the backside of the Shin-Etsu wafers (stress-relief) may be related to the device performance.

SECTION III
DARK CURRENT DEFECTS IN CCD IMAGERS ON CONTROLLED MATERIAL

A. Experimental

Silicon wafers of several types were used as starting material. Czochralski material was obtained from the Silicon Material division of Texas Instruments with specifications as listed in Table 3. Wafers of each group were taken from the same boule. To determine the position in the boule from which the slice was taken, a diagonal notch was cut on the flat before the boule was sliced. The position of the notch on the flat thus determined the position of the slice in the boule.

In addition to the above material, float-zone material was obtained from Wacker Chemtronic with the same specifications as Group 1. To minimize the effects that variations in polishing might have on the density of dark current spikes, the float-zoned slices were subjected to the same polishing procedure used for the Czochralski material.

Backside damage was applied in two ways. On some slices half the backside was masked off using black wax, and backside abrasion was applied using 100 μm glass beads. Other wafers were submitted to NRL for applications of Impact Sound Stressing (ISS)[1] by G. Schwuttke at IBM.

Imagers were then fabricated on the material using a standardized process (see Appendixes A and B). Materials from several groups were run in the same lot. In addition, several slices from a control lot were included to verify the consistency of the processing.

After processing, imagers that were functional were imaged, and the dark current maps of each imager were recorded. Those slices on which the yield was highest were selected for characterization of defects.

Table 3
Specifications for Subgroups of Wafers
from Varian Czochralski Crystals

Group #	Description
1	3 inch (7.62 cm) Varian Czochralski Resistivity = 8 to 15 Ω cm Boron doped Diameter = 2.985 to 3.010 inches (7.58 to 7.65 cm) Orientation = 1-0-0 ± 1° Etch pit count < 500 Lifetime > 30 μsec Flat orientation = 1-1-0 ± 2° Flat length = 0.9 to 1.1 inches (2.29 to 2.79 cm) Notch in flat. Depth = 0.032 inch (0.081 cm) 　　　　　　　　Width = 0.115 to 0.135 inch 　　　　　　　　　　(0.292 to 0.343 cm) Polished to 17 to 19 mils (0.43 to 0.48 mm) Taper = 1.5 mils (0.038 mm) Bow = 2.0 mils (0.051 mm)
2	Same as 1, except backside abrasion added
3	Same as 1, except Flat orientation = 0-0-1 ± 2°
4	Same as 1, except Orientation = 1-1-1 ± 1° Flat orientation = 1-1-0 ± 2°
5	Same as 1, except Orientation = 1-1-1 ± 1° Flat orientation = 1-1-2 ± 2°
6	Same as 1, except Diameter = 1.985 to 2.010 inches (5.042 to 5.105 cm) Orientation = 1-0-0 ± 2° Flat length = 0.5 to 0.6 inch (1.27 to 1.52 cm) Bow = 1.5 mils (0.038 mm)

For characterization, the overlying oxide aluminum and polysilicon were first removed by immersing the slices in an HF solution to which ascorbic acid had been added and through which nitrogen was bubbled. This was necessary to eliminate the strain interference from the superstructure that masks the strain pattern of the defects. Reflection and transmission x-ray topographs were then recorded from each slice. To maximize the resolution, each topograph was actually a series with the photographic plate placed as close as possible to the slice. At least one high resolution topograph was made of each slice using the elon-ascorbic acid developer described in Appendix D.

The imagers were then thinned using the procedure of Appendix E for examination in the transmission electron microscope. Earlier work was performed using a Siemens IA operating at 125 kV. Later work used a JEOL-100CX operating at 100 kV and equipped with a field emission gun, STEM attachment, and Kevex x-ray detector.

In addition to the controlled material, some additional devices were studied, and results are presented.

B. General Results

Some general results are discussed below, followed by the specific results for each material.

(1) It was observed that the general distribution and density of dark current spikes were consistent on material from the same group, but processed in different lots. This is indicative of a well-controlled process.

(2) Slices processed on (111) material had a very poor charge transfer efficiency. It was therefore impossible to successfully image these devices, and this portion of the experiments was not successful.

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(3) In general, a one-to-one correlation between dark current spikes and defects visible in x-ray topography was possible only when the total number of defects was small (< 10). As the defect density increased, very few of the defects were visible in x-ray topographs. This was a result of the small size or surface nature of the defect.

C. Results on Controlled Material
1. Czochralski - Group 6
a. Image Performance

This material group was significant because very few dark current spikes were visible on the imager. However, toward the edge of the slice, devices exhibited a banding in dark current. A dark current map typical of this banding is shown in Figure 2.

b. X-Ray Topography

Reflection x-ray topography showed the existence of bands of defects. A reflection topograph illustrating this is shown in Figure 3. This topograph is taken from the indicated portion of the imagers in Figure 2. Comparison of the dark current image and the topograph revealed a striking correlation between bands having a high density of defects in the topographs and bands of low dark current in the image, with a similar correlation between a low density of defects and high dark current.

A section topograph of this device is shown in Figure 4. It can be seen that the bands of defects in Figure 2 occur where a plane of defects in the bulk intersects the surface. In unpublished previous work we observed similar behavior in some material and concluded that the planes of defects were a result of the heterogeneous precipitation of oxygen onto defects grown into the crystal.
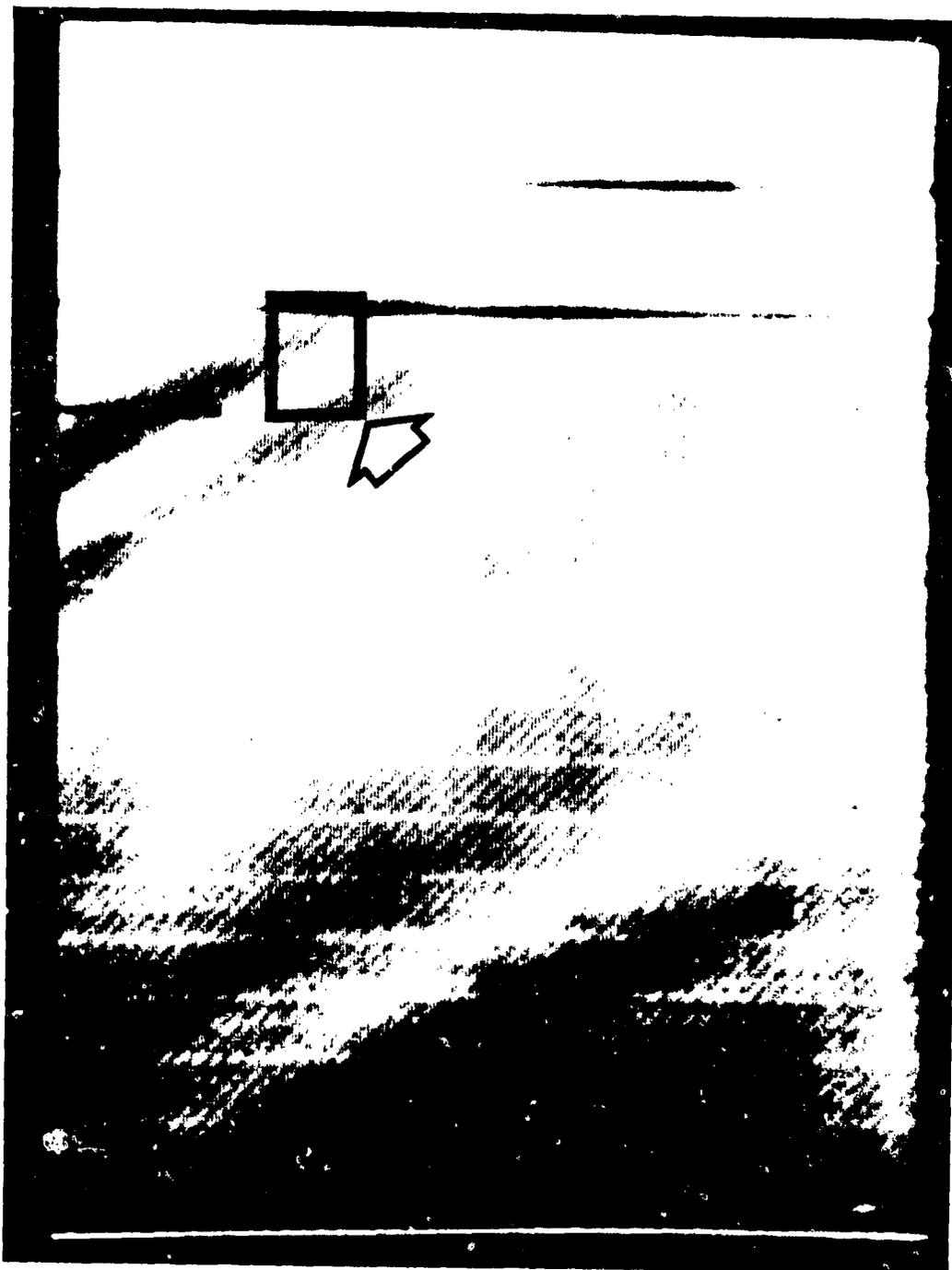
Figure 2 Dark Current Map of Device in Figure 3. Reflection topograph o
Figure 3 is taken at rectangle indicated by arrow.

Low Defect, High
Dark Current Region

High Defect, Low
Dark Current Region

Low Defect, High
Dark Current Region

High Defect, Low
Dark Current Region
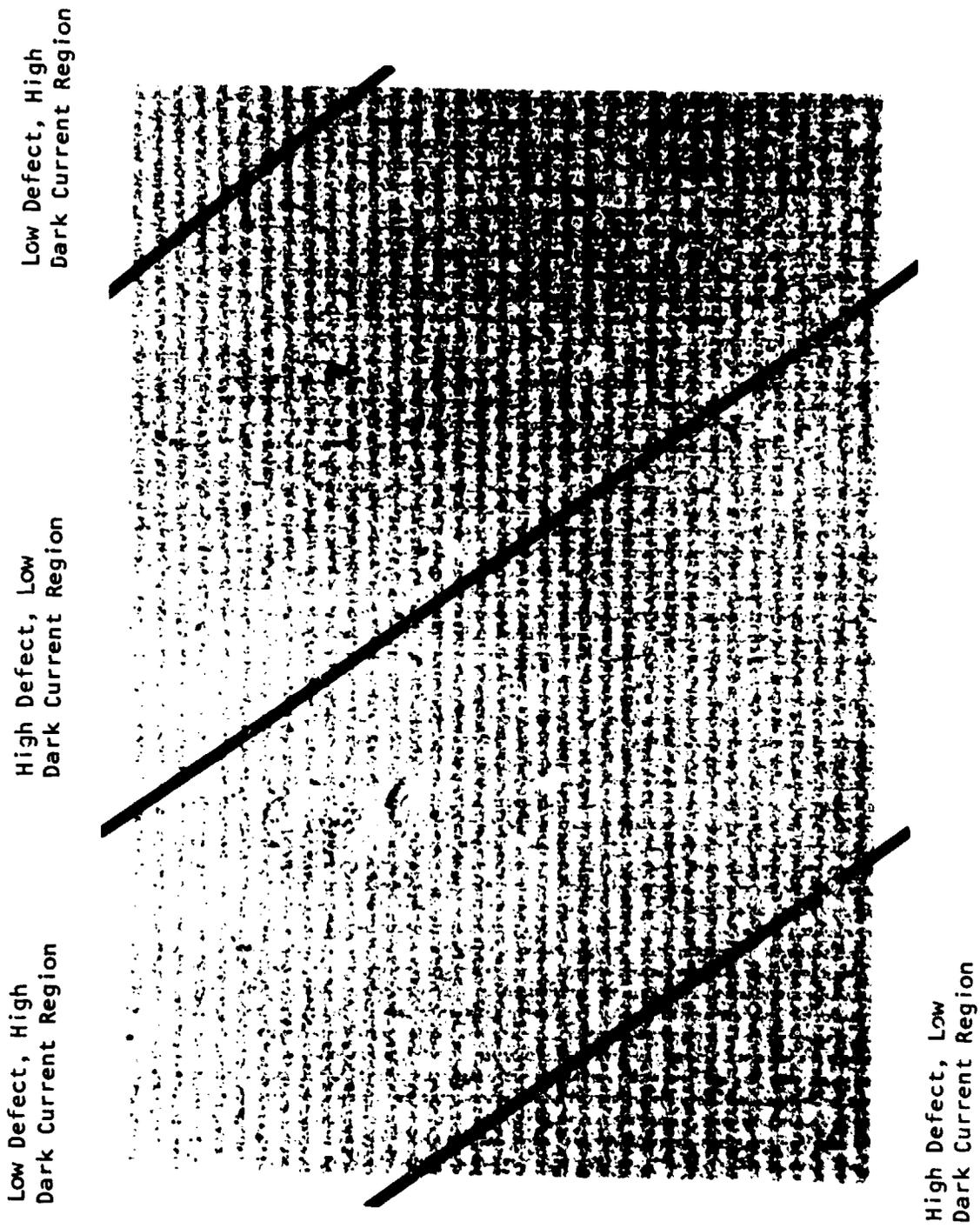
Figure 3   Portion of a $42\bar{2}$ Reflection Topograph of Device Exhibiting Banded Swirl
Pattern of Dark Current

Device Side

Top

Bottom

Region of Re-
flection Topo-
graph, Fig. 2

Figure 4 Section Topograph of Device Shown in Figures 2 and 3. Top and bottom marks correlate this figure with Figure 3. Regions of low dark current correlate well with regions where the bands of defects approach the device surface.

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c. **Transmission Electron Microscopy**

Transmission electron microscopy of this device revealed no defects to a depth of ~ 5 µm below the front surface of the device. This is significant, since 5 µm is the maximum depth of the depletion region in the channels of this device.

At about 5 µm, dislocations and stacking faults were seen. Typical examples of these are shown in Figure 5. The density of dislocation loops was ~ 100 per pixel ($\sim 10^7$ cm^{2}), while the density of stacking faults was ~ 1 per 30 pixels ($\sim 5 \times 10^3$ cm^{2}) in an ~ 1 µm thick sample taken from the high defect density regions of the material. No diffraction patterns could be obtained from any of the observed precipitate particles. The size and density of defects were found to be the same in regions under both the channels and the channel stops. The stacking faults, when imaged under conditions such that the stacking fault fringe should be out of contrast for a perfect stacking fault, revealed a residual fringe contrast (Figure 6). This is indicative of an adsorbed impurity on the stacking fault (see Section V).

d. **Discussion**

Dislocation loops in similar material have been reported by Tice and Tan[2,3] and by Schwuttke.[4] They concluded that the dislocation loops originated by prismatic punchng. Certainly Figure 5(c) is consistent with this assignment.

The stacking fault in Figure 5(a) is remarkable in that it has a precipitate particle at its center. Similar types of stacking faults have recently been reported and discussed by Maher, et al.,[5] and by Patel, et al.[6]

It has also recently been reported[7] that bulk swirl precipitation similar to that seen in this study can be initiated by a double heat treatment, with the first heat treatment greater than 820°C. To

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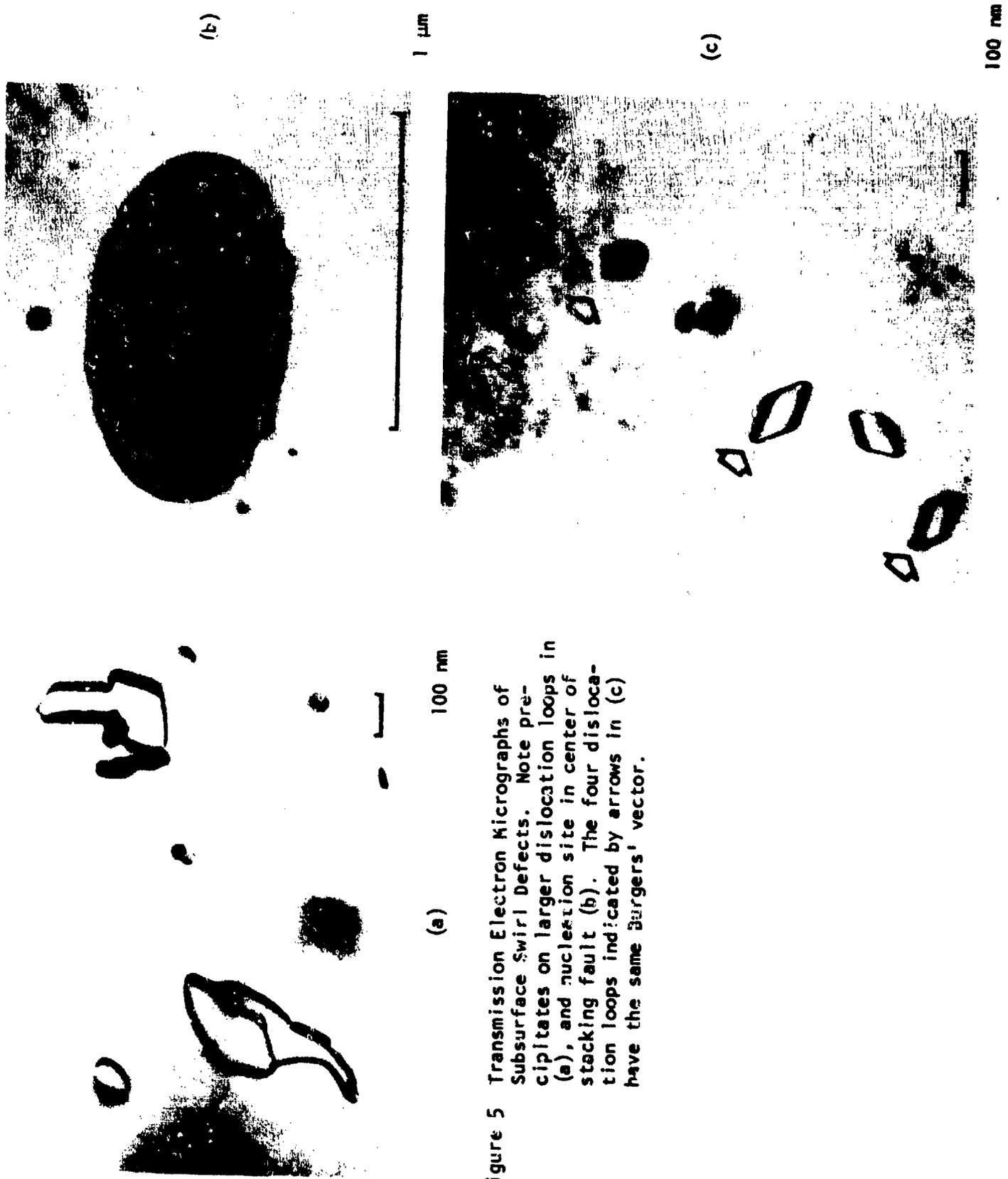
Figure 5 Transmission Electron Micrographs of Subsurface Swirl Defects. Note precipitates on larger dislocation loops in (a), and nucleation site in center of stacking fault (b). The four dislocation loops indicated by arrows in (c) have the same Burgers' vector.

$\vec{g} = 131$

$\vec{g} = 220$

500 nm
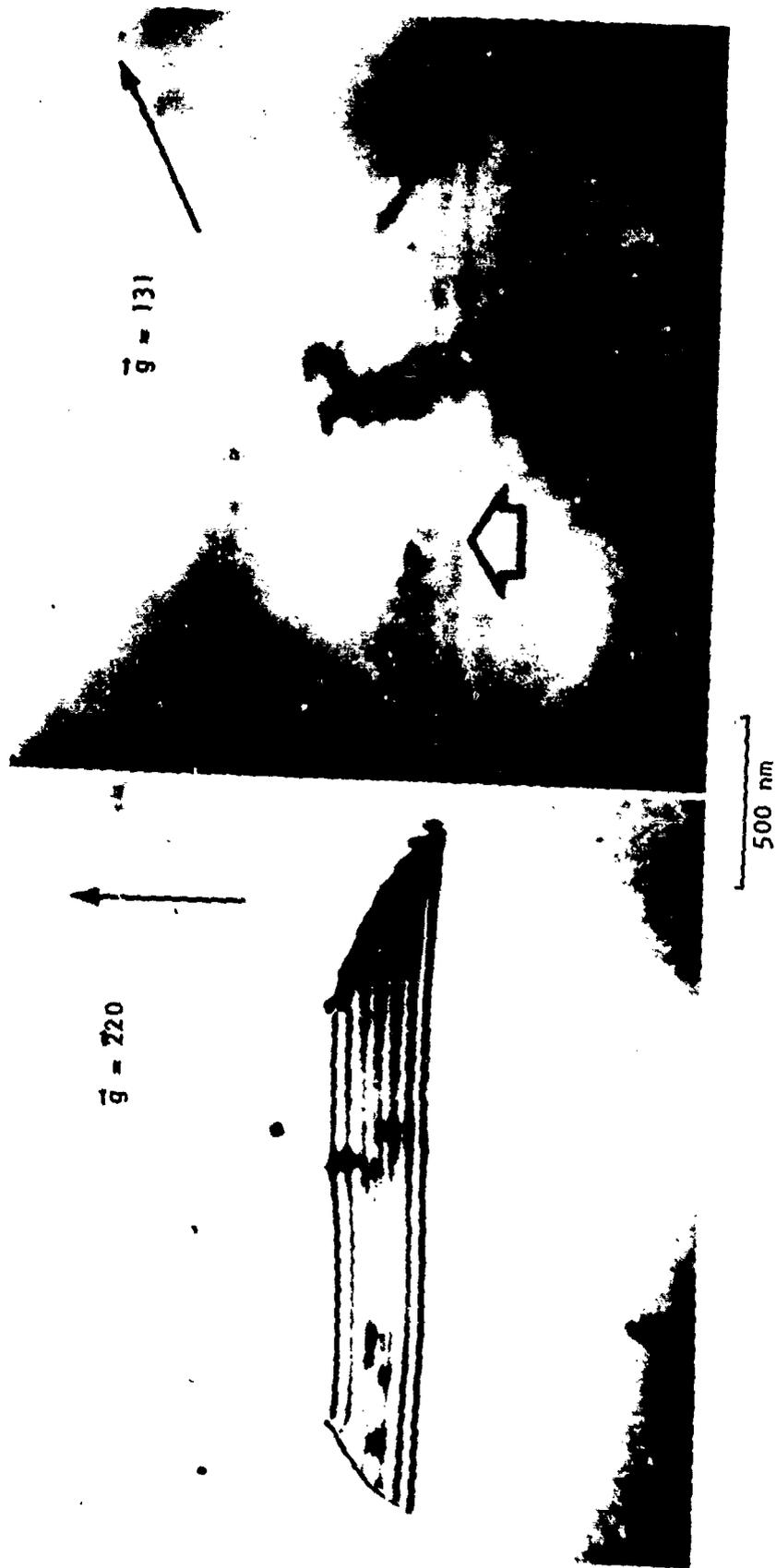
Figure 6 Stacking Fault Underneath a Channel. Residual contrast (open arrow) when $\vec{g} = 131$ shows stacking fault has an adsorbed impurity.

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understand the occurrence of this precipitation in our devices, some additional experiments were performed. First, a series of slices was processed, with two being pulled after each high temperature step. Subsequently, all slices were studied using transmission x-ray topography. It was found that the precipitation was not visible after boron channel stop deposition, but prior to the boron drive/thick oxide growth step; however, it was visible in the topographs after the boron drive/thick oxide growth. Additional experiments were performed at 1000°C. By study of transmission x-ray topographs, it was observed that the precipitation was visible after a one-hour/withdrawal/two-hour cycle, but not when the material was left in the furnace the entire three hours. It is not clear exactly what is happening during the cooldown, but it seems reasonable to assume that prismatic punching occurs, followed by accelerated precipitation on the dislocations during the subsequent heat treatment. This would explain the precipitates on dislocations in Figure 5(a).

The fact that the size and density of defects are independent of whether or not the defects are under the channel/channel stop indicates that the diffusion constant of the species that transports excess interstitials from the oxide silicon interface is either very long (to affect all defects) or very short (to affect none). Specifically, the diffusion length must be either less than 5 μm or considerably greater than 20 μm during the process cycle (nine hours at 1000°C).

It is interesting to note that if we assume that the defect-free region immediately below the surface is established during the initial oxidation, then the diffusion length of the out-diffusing species is close to that of oxygen, as reported by Yue, et al.[8]

The observed dark current banding is evidently of atomic dimensions or is a surface defect, since no defects have been observed with

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the electron microscope to correlate with this banding. The observed
anti-correlation between high dark current levels and subsurface defects is
indicative, however, of a short-range (< 50 μm) gettering mechanism.

2. Czochralski - Control Group

These slices were taken from a group of control material to
determine the consistency of the processing.

a. Imager Performance

A typical dark current pattern observed in devices made on this
material is shown in Figure 7. The random distribution of dark current spikes
illustrated in this figure is typical of all imagers that were operated on the
slice.

b. X-Ray Topography

Very few defects were imaged in both reflection and
transmission x-ray topography. Consequently, there is no correlation between
the predominant dark current producing defect and defects visible in x-ray
topography. However, transmission topography showed that the bulk of the
slice contained a uniform "swirl" precipitate (Figure 8).

c. Transmission Electron Microscopy

Samples for transmission electron microscopy were taken from
regions of imagers that showed the highest density of defects. Typical
defects seen in this material are illustrated in Figure 9. Stacking faults
[Figures 9(a) and 9(b)] were seen only in the channel stops. Approximately
90% of these stacking faults were found to be located underneath the
polysilicon gate (Figure 10). The length of the stacking faults varied from
approximately 0.5 μm to 10 μm. Most were under 1 μm in length. No
precipitates were observed on any of these faults. Dislocation loops were
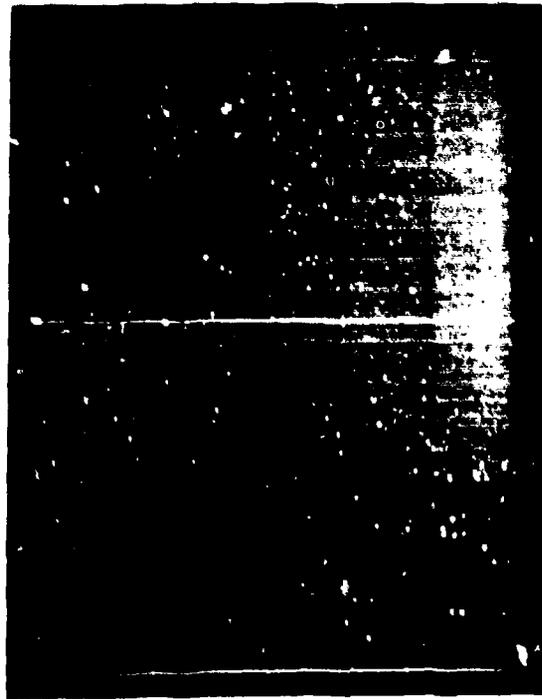
Figure 7   Dark Current Patterns: Czochralski - Control Group

Figure 8 (220) Transmission Topograph of Wafer from Czochralski - Control Group.
Note dark swirl precipitation region covering most of the slice.

Figure 9 TEM Micrographs of Defects in Czochralski – Control Group Devices. (a) and (b), stacking faults in channel stops; (c) and (d), dislocations in channels. All markers = 0.5 μm.

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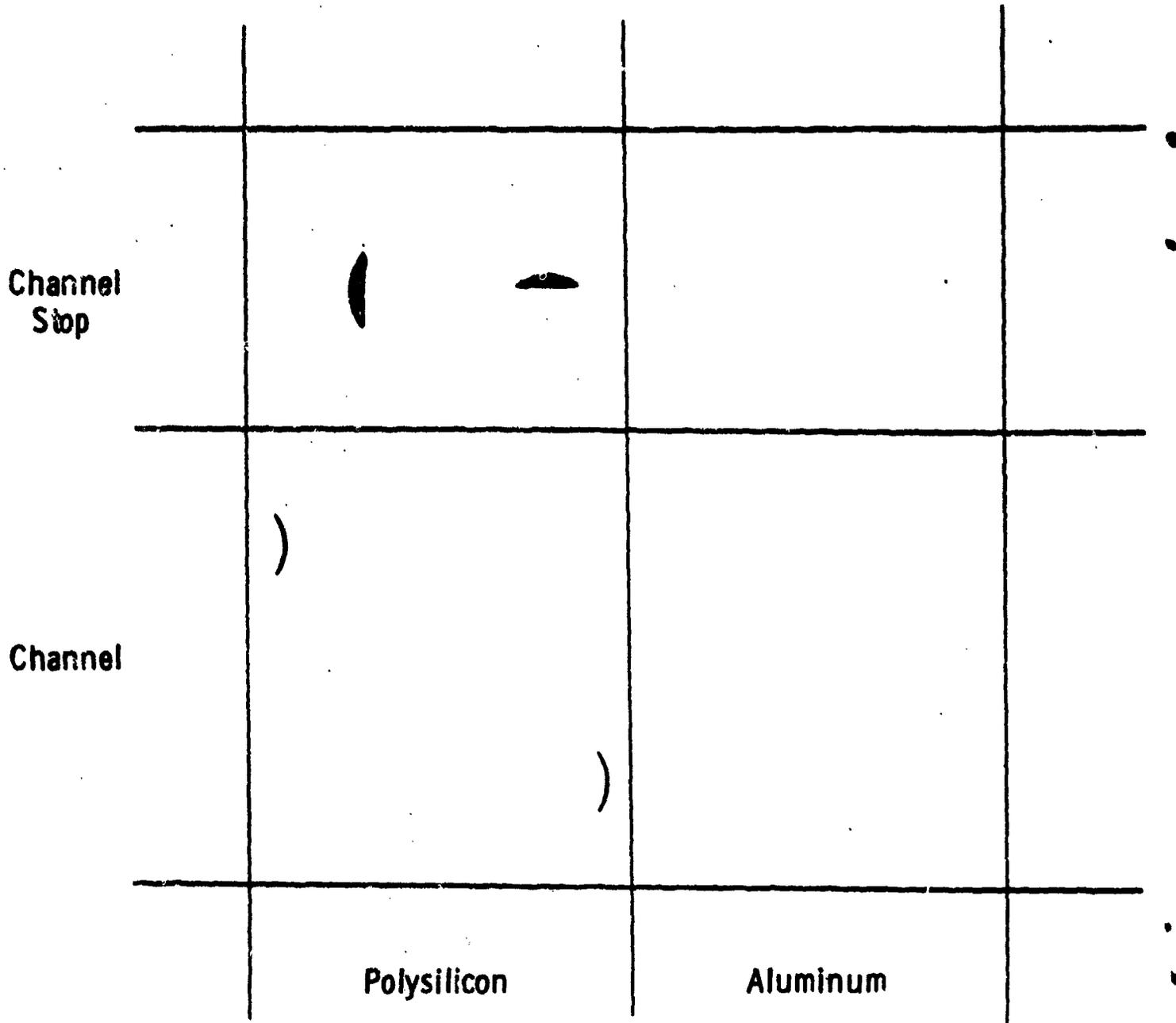
Figure 10   Distribution of Defects in Czochralski - Control Group.   Stacking
faults in channel stops, and dislocation loops in channels, both
predominantly under the polysilicon electrode.

found in both the channels and channel stops. These loops were invariably oriented in a ⟨110⟩ direction. In the channels they were found to be oriented only in a direction perpendicular to the channels and channel stops. All the dislocations in the channels were found at the edge of the polysilicon gate (Figure 10). In the channel stops they were oriented either in this same direction or in a direction perpendicular to the channels and channel stops. Contrast experiments in the electron microscope showed that all these dislocations were pure edge dislocations [i.e., the Burgers vector was perpendicular to the dislocation line, and in the (001) plane of the surface of the slice]. Furthermore, these experiments showed the dislocation surrounds an interstitial plane of atoms inserted from the oxide/silicon interface. The density of the dislocations in the channels was found to be approximately the same as the density of dark current spikes in the imager. The density of stacking faults in the channel stops was considerably larger. (To date, we have observed six dislocations in the channels, and approximately 30 stacking faults and dislocations in the channel stops.)

Weak beam experiments were conducted on some of the dislocations in the TEM. Typical results are shown in Figure 11. These defects were found in the channel stops. The ends of the dislocations were frequently found to be dissociated on a (111) plane containing both the Burgers vector and dislocation line. The traces of these planes on the surface of the sample are perpendicular to the projection of the dislocation line.

A weak beam micrograph of a typical dislocation in the channel is shown in Figure 12. Only the end of the dislocation was generally found to be dissociated.

No precipitates were observed in any samples. X-ray analysis in the STEM mode showed no detectable impurities on any of the defects.

$\vec{g} = 220$

(b)

$\vec{g} = 2\bar{2}0$

(c)

50 nm

$\vec{g} = 400$

(a)
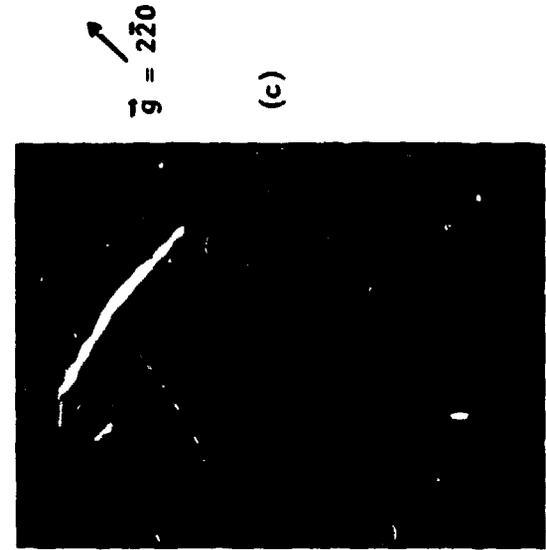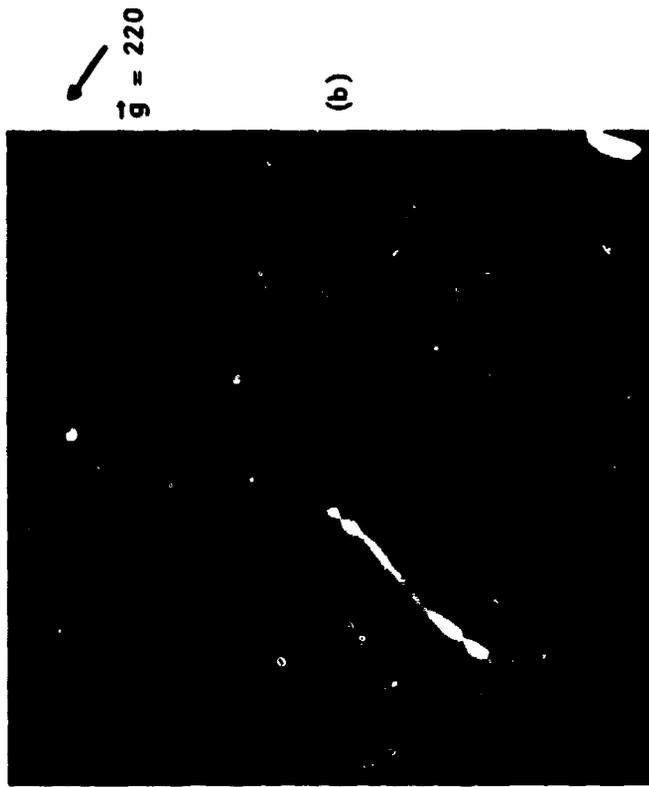
Figure 11 Dislocations in Channel Stops.
(a) Bright field, (b) and (c)
weak beam. Portions of the
long dislocation line are
dissociated.

50 nm

Figure 12 Weak Micrograph of Edge Dislocation in Channel. Only the end is dissociated.

d. Discussion

This discussion will be confined to the origin of the stacking faults and dislocations. Although it certainly appears that the small dislocations are the source of dark current spikes in these devices, discussion of the reason this is so will be postponed until Section VI.

Dislocations such as those seen in Figure 9 cannot originate by a simple glide mechanism; that is, they cannot originate at some point in the crystal and move by slip to their present position because the plane containing both the dislocation line and the Burgers vector of the dislocation is a (100) plane and not a slip plane, which must be of the type (111). There are three mechanisms by which these pure edge dislocations may form: (1) through the unfaulting of a stacking fault, (2) through the formation of the dislocation at the surface and the subsequent climb of the dislocation by the emission or absorption of silicon interstitials or vacancies, and (3) through a dislocation reaction such as $\frac{1}{3}\langle 10\bar{1}\rangle \rightarrow \frac{1}{6}\langle 1\bar{1}0\rangle + \frac{1}{6}\langle 01\bar{1}\rangle$. Of these mechanisms, the first seems the most probable. In Section V, where the unfaulting of stacking faults is studied, it is concluded that immediately after the unfaulting process, if the Shockley partial is nucleated at the surface intersection of the Frank partial, the defect that should be observed is a dislocation in a predominantly $\langle 110\rangle$ direction with Burgers vector $\frac{1}{2}\langle 1\bar{1}0\rangle$ surrounding an interstitial plane of atoms. Both of these criteria are met by all of the dislocation loops we have studied. We conclude that the defects seen in this material originate from the same source, namely, the growth of a stacking fault.

The origin of the stacking fault is less clear. Certainly, the almost circular stacking fault with no precipitate in the center shown in Figure 9(b) is indicative of a subsurface bulk origin (see Section V). That most of the defects are of comparable size further supports that they are also nucleated from a subsurface bulk mechanism. The small size, however, suggests

30

that they are nucleated late in the process, i.e., after thick oxide growth. Section V presents data that suggest these subsurface stacking faults are nucleated by trace amounts of copper.

As depicted in Figure 10 the distribution of defects, which is device dependent, could arise from a device-dependent nucleation mechanism, or a random nucleation mechanism, and a device-dependent annihilation mechanism. With the data at hand, it is impossible to distinguish which of these two mechanisms is at work, and plausible arguments for either may be made. If copper is, in fact, the nucleating agent of the stacking faults, then it is possible that the distribution of copper near the surface is device-dependent. Section V presents evidence that the source of copper for one mode of precipitation is the surface. If the amount of copper at the surface were a function of the thickness of the oxide and the presence of the overlying polysilicon, then the distribution of defects could be explained. An additional role played by the edges of the polysilicon would be to stress-assist the unfaulting of the stacking fault, eliminating all stacking faults in this region.

Alternatively, the stacking faults could nucleate and grow in all portions of the device, but the processing of the device could favor the removal of the stacking faults in some portions of the device by either a shrinkage or an unfaulting mechanism, with subsequent climb of the resulting perfect dislocation out of the crystal. The role of the thick oxide, particularly when it is overlain by polysilicon, would thus be to inhibit the unfaulting of the stacking faults. In the channel where the oxide is always relatively thin, the unfaulting would evidently occur with comparative ease, and the resulting perfect dislocations would be able to climb out of the silicon.[9] The driving force for the climb process would be the image force induced by the surface. At the edges of the polysilicon, the strain field

31

from the polysilicon is evidently sufficient to inhibit the climb of the dislocations, and it is here that we see the dark current producing defect.

That the resulting perfect dislocations in the channels are not dissociated is in agreement with theory. The only energetically favored dissociation of a perfect dislocation is into two Shockley partials: $1/2\langle 110\rangle \rightarrow 1/6\langle 21\bar{1}\rangle + 1/6\langle 121\rangle$. For this reaction to occur, the dislocation line and the Burgers vector of the dislocation must lie on a slip plane. This is the case only for the ends of some of the dislocations, as has been discussed.

3. Float-Zoned Material

a. Imager Performance

Dark current patterns from imagers on float-zoned material fell into two distinct categories. Devices in the central region of one slice and about the periphery of all slices showed dense patches of dark current lines running in $\langle 110\rangle$ directions on the slice [Figure 13(a)]. Devices outside of these regions showed a moderately low density of randomly distributed isolated dark current spikes [Figure 13(b)].

b. X-Ray Topography

The wafer containing the center patch of dark current was selected for study by x-ray topography and transmission electron microscopy. Transmission topographs of this wafer showed that the center patch of dark current was caused by dislocations introduced from the backside of the wafer (Figure 14). Comparison of this topograph with others taken on other slices processed in the same batch showed that the origin of the backside damage was in the process, evidently during a photoresist spinning operation. In contrast to the float-zoned slice, the dislocations induced in the Czochralski slices were confined to the backside and did not propagate to the front surface. It should be noted that the process used has been optimized for

32
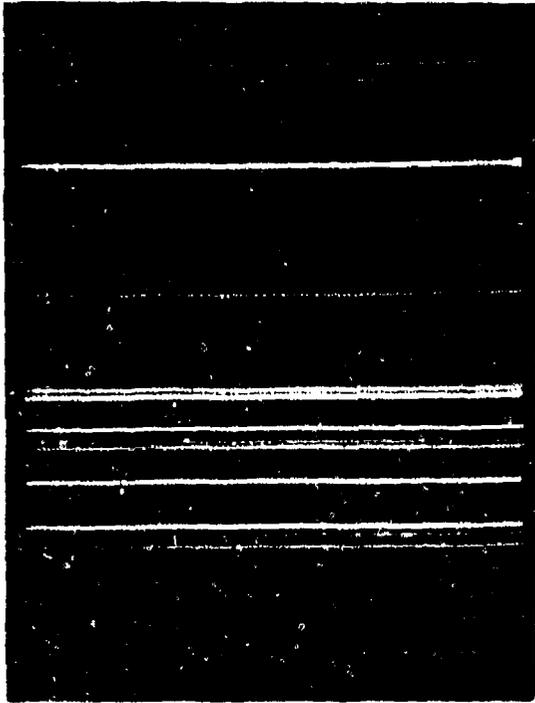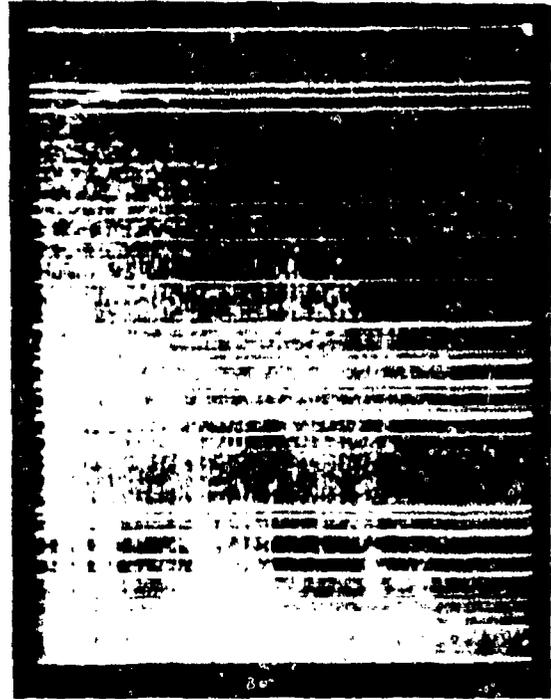
(a)   (b)

Figure 13   Dark Current Patterns – Float-Zoned Group

33

Figure 14   (220) Transmission Topograph of Float-Zoned Wafer Showing Damage Near Center.   Vertical bars result from action of automatic Bragg angle control.

Czochralski wafers. Enlargements made from the transmission topographs show the propagation of the dislocations from the backside to the frontside (Figure 15).

The damage introduced in the backside was sufficiently great that the warpage of the slice precluded making a reflection topograph of the entire frontside of the slice. In regions where the backside damage was severe, a large density of dislocations was found in the reflection topographs (Figure 16). In the imager array it was found that these regions correlated well with the regions of dense dark current. There was not a one-to-one correlation between dislocations seen in the topographs and dark current spikes outside this region, however. That is, many dislocations did not act as dark current sources. In regions outside the dislocation patches, no defects were imaged on either transmission or reflection topographs that correlated with the random, moderately low density of dark current spikes reported above.

c.   Transmission Electron Microscopy

In samples taken from devices near the center of the slice, long lengths of dislocation line, very close to the surface, were found to be oriented either parallel or perpendicular to the channels and channel stops. Contrast experiments show that all these dislocations are of the 60 type, i.e., their Burgers vectors are in $\langle 110 \rangle$ directions that do not lie in the plane of the surface (Figure 17).

Occasionally, we find that a dislocation reaction has occurred. Figure 18 illustrates an example where two dislocations having the same Burgers vector, but lying on two different (111) planes (the traces of which are perpendicular in this figure), intersect.

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Figure 15 Enlargement of (220) Transmission Topograph Showing Dislocations Emanating from Backside-Damaged Regions

0.5 mm

36

Figure 16 Enlargement of (224) Reflection Topograph of Dislocated Region in Float-Zoned Region

0.5 mm

Polysilicon   Aluminum

Channel

Channel Stop

5 μm

Figure 17   Transmission Electron Micrograph of 60° Dislocations Near Front
Surface of Float-Zoned Wafer

100 nm
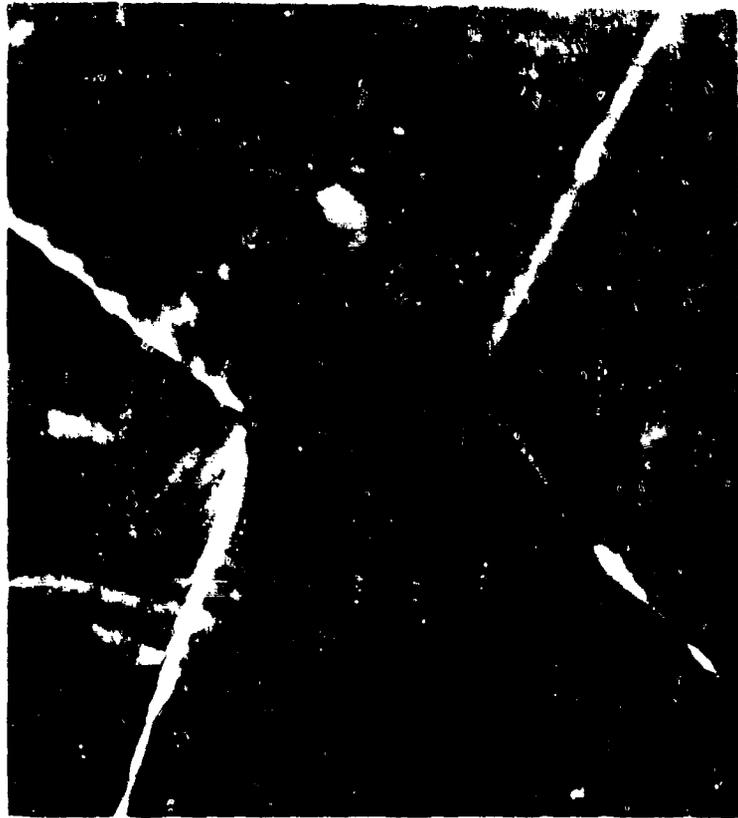
Figure 18   Dark Field Transmission Electron Micrograph of Float-Zoned Wafer Showing Dislocation Reaction. Two perpendicular 60° dislocations moving on two different slip planes, but with the same Burgers vectors, have reacted to form nearly right-angle configuration.

39

Three of these dislocations have been examined using the weak beam method. All these dislocations were found to be extensively dissociated; a typical example is shown in Figure 19. The separation at A in this image is 65 Å. Since the partial dislocations lie on an inclined (111) plane, their true separation is approximately 100 Å. At B in this same figure the dislocations also appear to be dissociated by approximately 50 Å. At C there is a constriction where the dislocation is not dissociated.

In addition to the dislocations, a small number of small stacking faults was observed in the channel stop (Figure 20). All the stacking faults were of the same length.

Samples were also taken from devices exhibiting the moderate density of low level dark current defects. A typical example of the defects found in these regions is illustrated in Figure 21. Here we see a dislocation in the channel and a stacking fault in a neighboring channel stop. Contrast experiments showed that all dislocations were of pure edge character. The density of dislocations in the channels correlated well with the density of dark current spikes in the portion of the imager from which the sample was taken.

STEM x-ray analysis of both dislocations and stacking faults showed no detectable impurity.

d.   Discussion

The long length of dislocation line in the depletion region of the imager clearly originates by a glide process, with the dislocation originating on the back surface. The fact that the dislocation does not exit through the surface, but remains at a shallow depth, is evidently a result of the existence of the thermal oxide. The energy of the system would be lowered if these dislocations moved out through the front surface. For a clean

30 nm
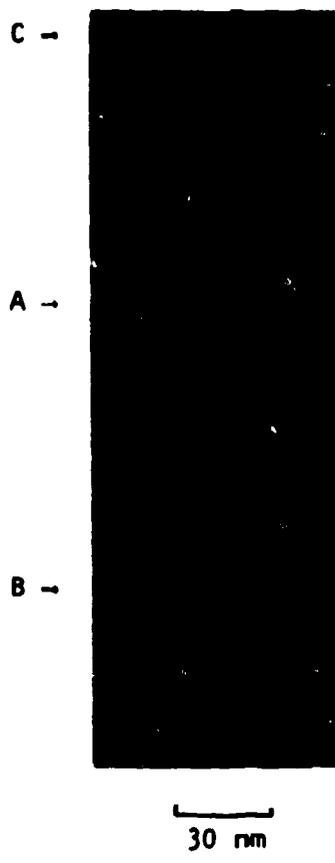
Figure 19   Weak Beam (400) Micrograph of Partially Dissociated Dislocation.
Separation in image at A is 6.5 nm, 3.5 nm at B, and no dissociation
at C.

0.5 μm

Figure 20   Transmission Electron Micrograph of Stacking Fault in Channel Stop
of Float-Zoned Wafer

0.5 μm

Figure 21   Stacking Fault in Channel Stop and Dislocation in Channel

surface, image forces would also tend to pull the dislocation out of the silicon crystal. There must therefore be an inhibiting force caused by the presence of the thermal oxide.

The dissociation in Figure 19 proceeds according to the reaction. $1/2\langle 101 \rangle \rightarrow 1/6\langle 211 \rangle + 1/6\langle 112 \rangle$. The two partial dislocations are separated by a stacking fault on the (111) plane. The Burgers vectors and dislocation line orientation of both the perfect and partial dislocations are also found in this same plane. A similar situation exists for any dislocation that is in a configuration to move by a glide process.

The equilibrium spacing of the partial dislocations in "pure" silicon, and with no applied stresses has been measured. For the 60° dislocation it is between 50 and 60 Å.[10,11] For this configuration the stacking fault is found to be intrinsic (i.e., the stacking sequence across the fault corresponds to the sequence that would occur if a plane of atoms were removed). At B in Figure 19 this is seen to be the case. The separation at A is anomalously high. There are three possible explanations for this: (1) The stacking fault is extrinsic in this region (i.e., the stacking sequence across the fault corresponds to that if an atomic plane were inserted). Partial dislocations separated by extrinsic faults have been reported to occur when the dislocation is close to the screw (or 0 orientation.[11] The extrinsic stacking fault energy is deduced to be lower than the intrinsic stacking fault energy and, hence, the separation of the partials is greater. (2) Oxygen could be adsorbed onto the stacking fault in this region, causing the stacking fault energy to be lowered. (3) A force from the surface of the device could be acting on the dislocation, causing one of the partials to be moved closer to the surface. We are unable at this time to distinguish which mechanism is at work.

The origin of the stacking faults and edge dislocations is evidently the same as that discussed for the Czochralski control group. The major difference appears to be the occurrence of the edge dislocations at the edge of, and parallel to, the channel. This would suggest that the stress field of the thick oxide also favors the unfaulting of the stacking fault in the channel.

4. Czochralski - Group I

    a. Imager Performance

Dark current defect patterns in imagers on this material fell into two classifications. Near the periphery of the wafer there was a high density of defects in a discernible pattern [Figure 22(a)]. Devices in the center of the wafer showed a very low density of dark current defects. These frequently extended over more than one pixel [Figure 22(b)]. These slices had backside mechanical damage by sandblasting with glass beads over half the slice. There was a slight reduction in the defect density for imagers over the backside damaged portion of the slice.

    b. X-Ray Topography

There was no correlation between the reflection topographs and the high density of dark current defects found near the periphery of the wafer. Near the end of the wafer, however, there was a nearly one-to-one correlation between dark current spikes and dislocation cluster defects observed in reflection topographs. Two typical examples of these are shown in Figure 23. In Figure 23(a) it will be seen that most of the dislocations are electrically inactive. Only the dislocation indicated by the arrows is a source of dark current. Similarly, the dislocations emanating from the round defect in Figure 23(b) were not dark current sources. The round defect was a very intense source of dark current and led to blooming down the channel and into several adjacent channels.

45
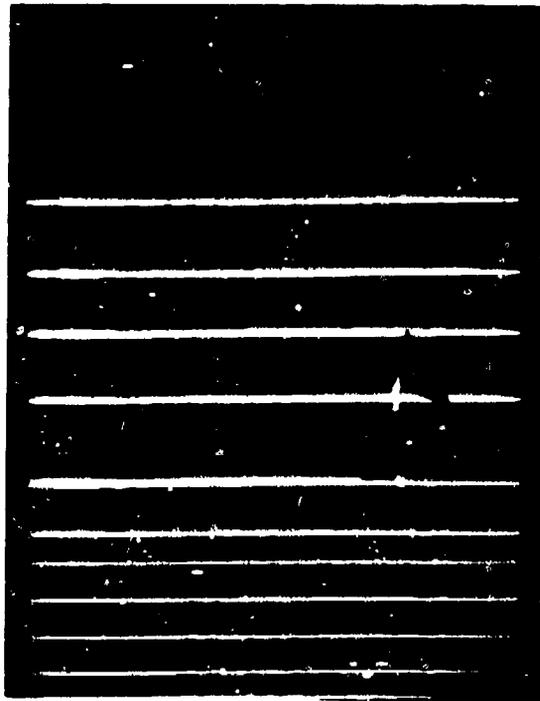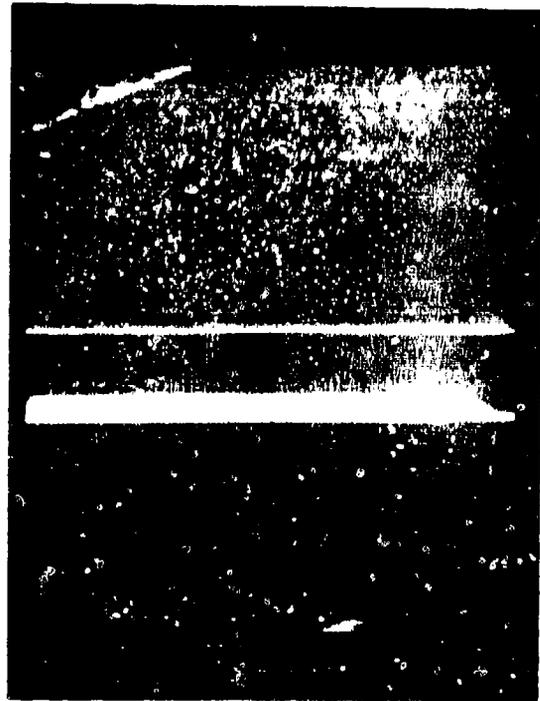
(a)   (b)

Figure 22 Dark Current Patterns - **Czochralski Group 1. Defect at arrow in**
(b) is shown in topograph, **Figure 23(a).**

(a)

(b)
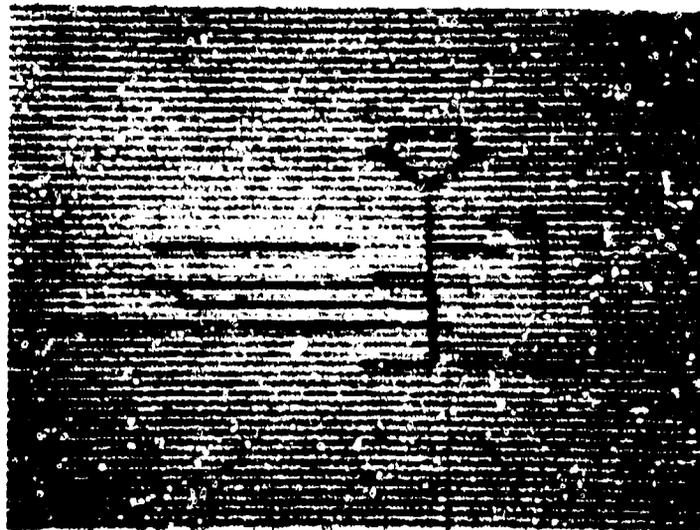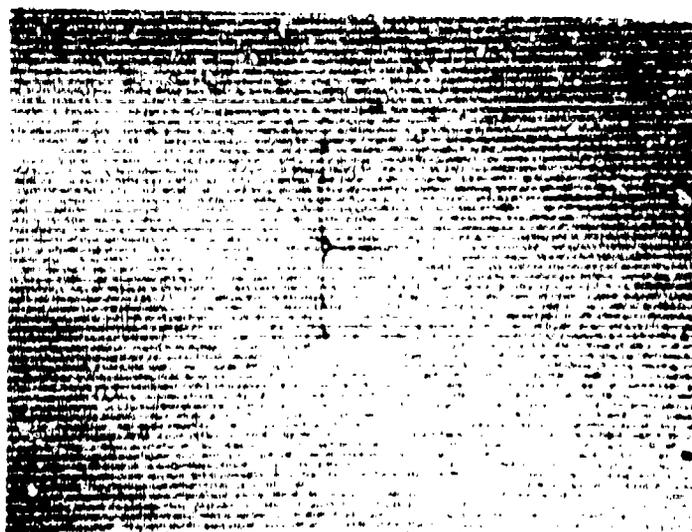
0.5 mm

Figure 23   (224) Reflection Topographs of Defects in Cznchralski Group I. Only
the dislocation indicated by arrow in (a) is a dark current source,
while in (b), only the spot in the center of the defect is a dark
current source.

47

Transmission topographs also showed that there was a region of bulk "swirl" precipitation near the center of the wafer. Devices lying over this swirl precipitation were those in which the density of defects was lowest.

5. Czochralski - Group 2
   a. Imager Performance
   The dark current spike behavior of this material was similar to that of Czochralski - Group 1. Imagers at the periphery of the slice had a moderately high density of weak dark current spikes, many of which were in a discernible pattern (Figure 24), while those near the center of the slice had a relatively low density of dark current spikes. Backside mechanical damage by glass bead sandblasting had no discernible effect on the dark current spikes.

   b. X-Ray Topography
   Only a few defects were imaged in reflection topography. These defects correlated with the more intense dark current spikes near the center of the slice. A typical example is shown in Figure 25, which correlates with the indicated dark current defect in device 3 of Figure 24. From the pattern of dark current defects of this type that were visible in the imagers and the topographs, it appears that their origin is frontside damage caused by handling of the slice before processing. (The backside damage was applied after the completion of the frontside polish.) No defects were imaged in reflection topography that correlated with the moderate number of dark current defects visible in some of the imagers.

   Transmission x-ray topographs showed that there was a region of bulk "swirl" precipitation in this material. There was a general, but not specific, correlation between the occurrence of this precipitation and imagers with low dark current defect density. Figure 26 is an enlargement of a
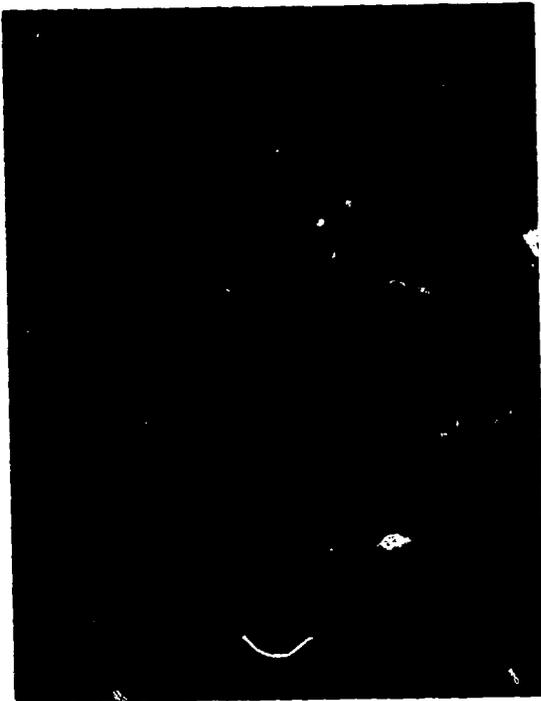
Device 1   Device 2
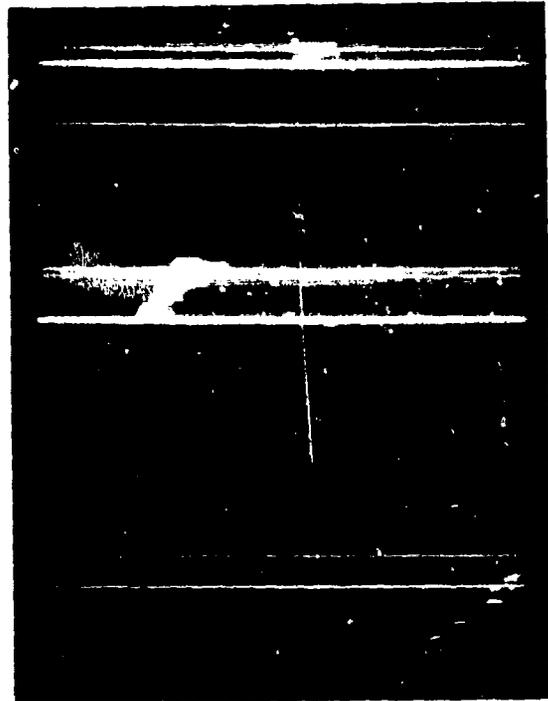
Device 3
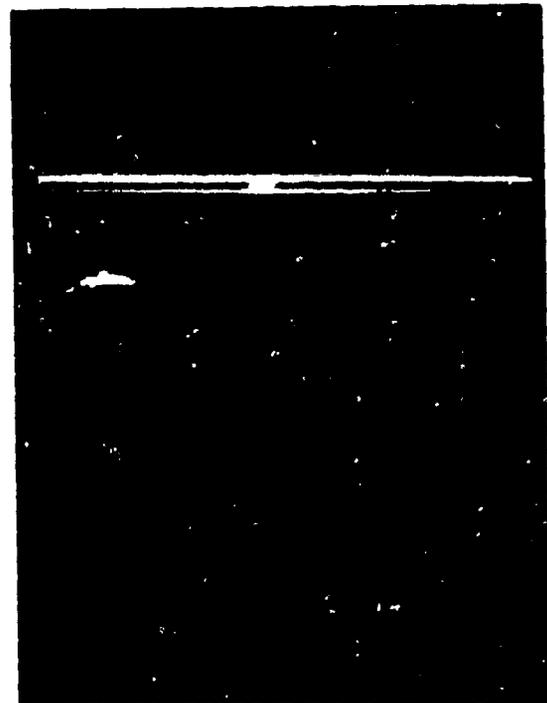
Figure 24 Dark Current Patterns of Three Adjacent Devices, Czochralski Group
           2.   Defect at arrow in device 3 is shown in topograph, Figure 25.

L____J
100 μm

Figure 25   2$\bar{2}$4 Reflection Topograph of Dark Current Defects in Czochralski
Group 2.   Defect is marked in Figure 24, device 3.
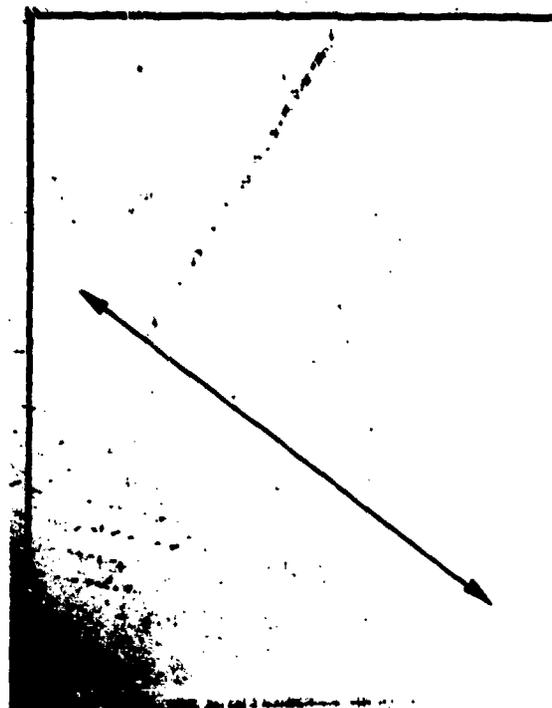
Device 1   Device 2

Figure 26   (220) Transmission Topograph of Two Devices Whose Dark Current
            Signature is Shown in Figure 24. Bulk swirl precipitation region
            is the darkening most noticeable in device 1. Arrow in device 2
            indicates line above which there are numerous dark current defects.
            Black spots and lines on topograph are defects on the backside of
            the devices.

transmission topograph of devices 1 and 2 of Figure 24. It will be noticed that the edge of the band of dark current defects visible in device 2 parallels the swirl band visible in the topograph. The band of dark current defects is offset from the edge of the swirl by approximately 1 mm, however.

c. Transmission Electron Microscopy

A sample for transmission electron microscopy was taken from the high defect region of device 2, Figure 24, in the upper right-hand corner of this device. No defects were observed in this sample, indicating that the dark current defects were produced by the interface defect more thoroughly investigated for Group 3 material.

d. Discussion

It is important to establish the exact relationship between the dark current spikes and the bulk "swirl" precipitates in this wafer. Two possibilities exist: (1) that the swirl precipitate serves as a "getter" for these defects, or (2) that the growth conditions in the boule favor defect formation outside the region of the swirl, while slightly different growth conditions lead to a suppression of defect nuclei in the region of the swirl. If the former were the case in this wafer, then comparison of the transmission topograph and device 2 of Figure 24 shows that the "gettering" range of the swirl is of the order of 1 mm. Now in device 1 of this same figure there are also several defects with the same dark current characteristics. Reference to the transmission topograph, Figure 26, shows that these defects lie over a region of swirl precipitate that is somewhat less intense than the most intense regions, but still considerably more intense than the swirl precipitation within 1 mm of the band of defects in device 2. In addition, these defects lie within 1 mm of the most intense swirl regions. If these defects in device 1 are in fact the same as the defects in device 2, as seems most probable, and if a gettering mechanism were at work, then the defect in device 1 should be absent. The distribution of the dark current defects in

this slice thus appears to be a result of varying growth conditions in the boule when the crystal is grown.

6. **Czochralski - Group 3**

   This group had a ⟨100⟩ flat.

   a. **Imager Performance**

   Imagers on this material behaved similarly to imagers on Groups 1 and 2 in that those at the periphery of the wafer had a high density of dark current defects, while those near the center had a much lower defect density. There were several significant differences, however. The density of defects in some imagers was extremely high: of the order of 10% of the pixels had dark current spikes. In addition, the density of defects near the center of the slice was higher than for devices from the center of Groups 1 and 2. In some cases, there was a definite "swirl" pattern to the dark current spikes (Figure 27). Backside mechanical damage by glass bead sandblasting appeared effective in removing a large number of dark current spikes. For example, while the worst-case imagers on the undamaged side of the slice had approximately 10% of their pixels with a dark current spike, on the damage side the worst case was 1%.

   b. **X-Ray Topography**

   No defects were imaged in reflection topography on this material. Transmission topographs showed that this material also contained a central region of bulk "swirl" precipitate.

   c. **Transmission Electron Microscopy**

   Samples for transmission electron microscopy were taken from the central high defect regions of the imagers illustrated in Figure 27. No defects were imaged. These same samples were successively etched-back from the front surface in 2 μm increments and again examined in the electron
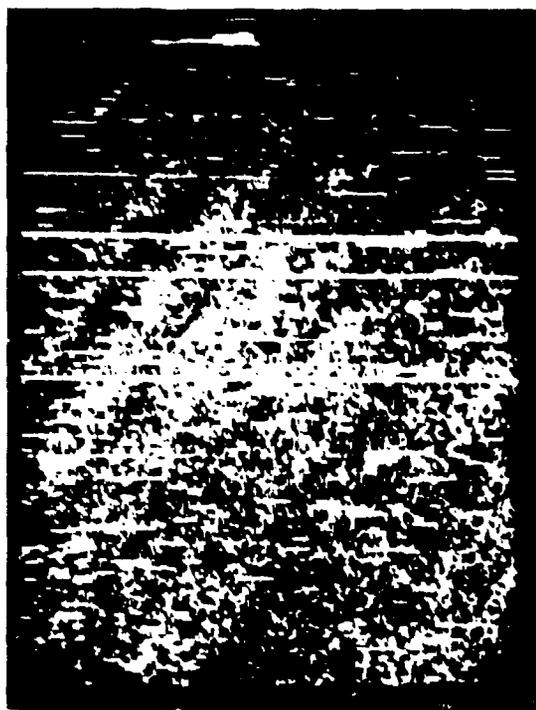
Figure 27 Dark Current Pattern in Czochralski Group 3

microscope. This procedure showed there were no defects in the outer 5 μm of the devices.

Samples taken from high defect regions of other devices had the dislocation clusters and stacking faults shown in Figure 28. Contrast experiments in the electron microscope showed that the long dislocation line in these clusters, which was oriented in a ⟨110⟩ direction, was of pure edge type. All these dislocation clusters were located in the channel stop.

An additional type of defect was seen in the channels (Figure 29). These defects were located underneath the aluminum electrode and primarily near the edge of a neighboring polysilicon electrode.

d. Discussion

The fact that the defects that cause dark current spikes were not imaged in the electron microscope sugests that they reside at the oxide/silicon interface. To our knowledge, only one such defect has been reported to date: a dislocation that results from the unfaulting of a stacking fault and that climbs out of the silicon to the interface.[12] It would be expected in our samples that if such were the case, some faulted or unfaulted stacking faults would be left behind. In fact, we see no defects in this high dark current spike region, either in the channels or in the channel stops. Since this defect does respond to backside gettering, it would appear that a most likely candidate for it would be an interfacial impurity.

The dislocation clusters that appear (Figure 28) are evidently slightly more complex versions of the same unfaulted stacking fault we have seen in other slices. The other defects (Figure 29) are apparently etch artifacts. We have been unable to correlate them with electrical activity. They are generally visible only in relatively thin regions of the sample, and

55

g = 220

g = 2̄20

0.5 μm

Figure 28   Dislocation Clusters in Channel Stop Region.   The longer dislocation lines are pure edge.

56
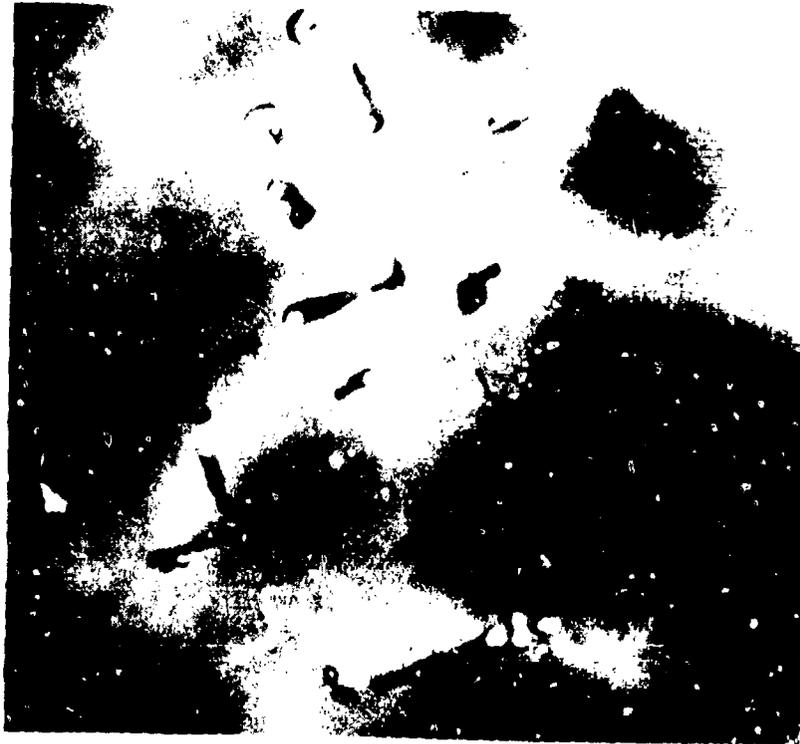
100 nm

Figure 29   Defects in Channel Region. The defect lines are oriented in ⟨100⟩
            directions.

only when the sample is tilted close to the Bragg angle for the reflection under study.

D. Results of Defect Studies in Other Devices

1. Dislocations

A series of dislocations was found in one device. Two of the dislocations were dark current sources (the only dark current sources), while the remainder were not. Reflection topographs of the two dark current sources are shown in Figures 30 and 31, while two typical non-dark-current sources are illustrated in Figures 32 and 33. It will be seen that the dislocations that are dark current sources lie in the channel stop (Figure 31), while the dislocations that are not dark current sources lie in the channels. The contrast behavior of all dislocations in reflection topography shows them to be 60° dislocations. Transmission topography shows that all of the defects have been nucleated by surface sources. They are found only in the array region, and hence are associated with the stress field of the device superstructure.

It is somewhat surprising that a dislocation located in a channel stop can act as a dark current source. That this dislocation is shallow can be deduced from Figure 34. Here it will be seen that part of the dislocation underneath a polysilicon layer has evidently been pulled out of the surface. Additional evidence for this interpretation is shown in Figure 35, where a large amount of segmentation can be seen, resulting from the strain field of the overlying polysilicon.

The fact that a shallow dislocation in the channel stop gives rise to a dark current spike is indicative of a shallow depletion region under the channel stop oxide. If a defect capable of producing dark current is located

58

$$\vec{g} = 422$$

(a)

⊢————⊣
100 μm

$$\vec{g} = 4\bar{2}\bar{2}$$

(b)
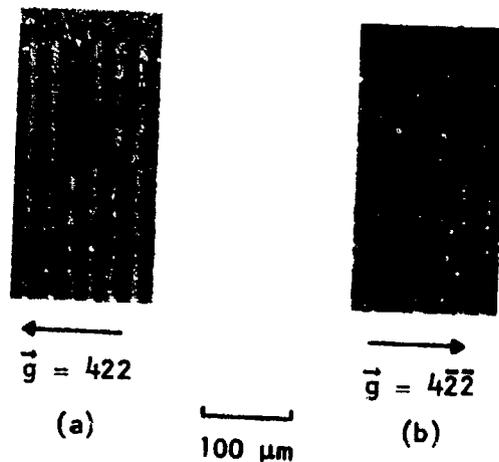
Figure 30 Reflection Topographs of Channel Stop Dislocations
That are Dark Current Sources

59

$\vec{g} = 422$

100 μm
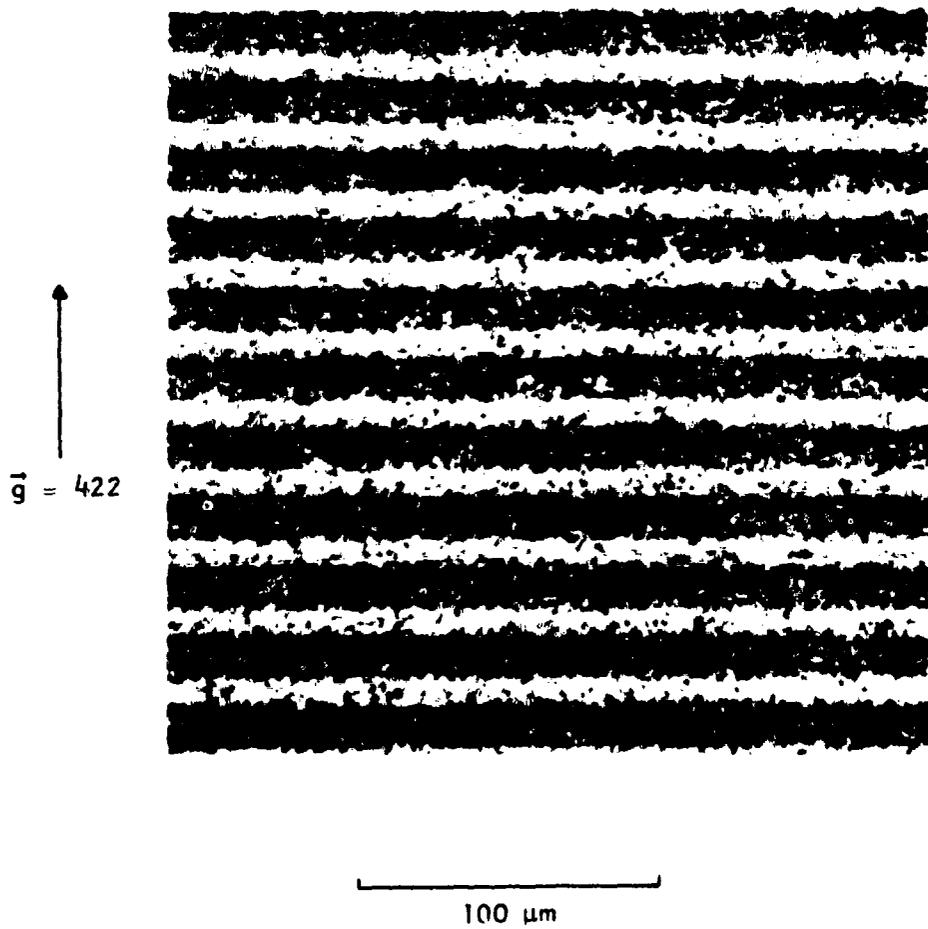
Figure 31   Topograph of Weak Dark Current Source

60

$\vec{g} = 422$

(a)

$\vec{g} = 4\bar{3}\bar{3}$

(b)
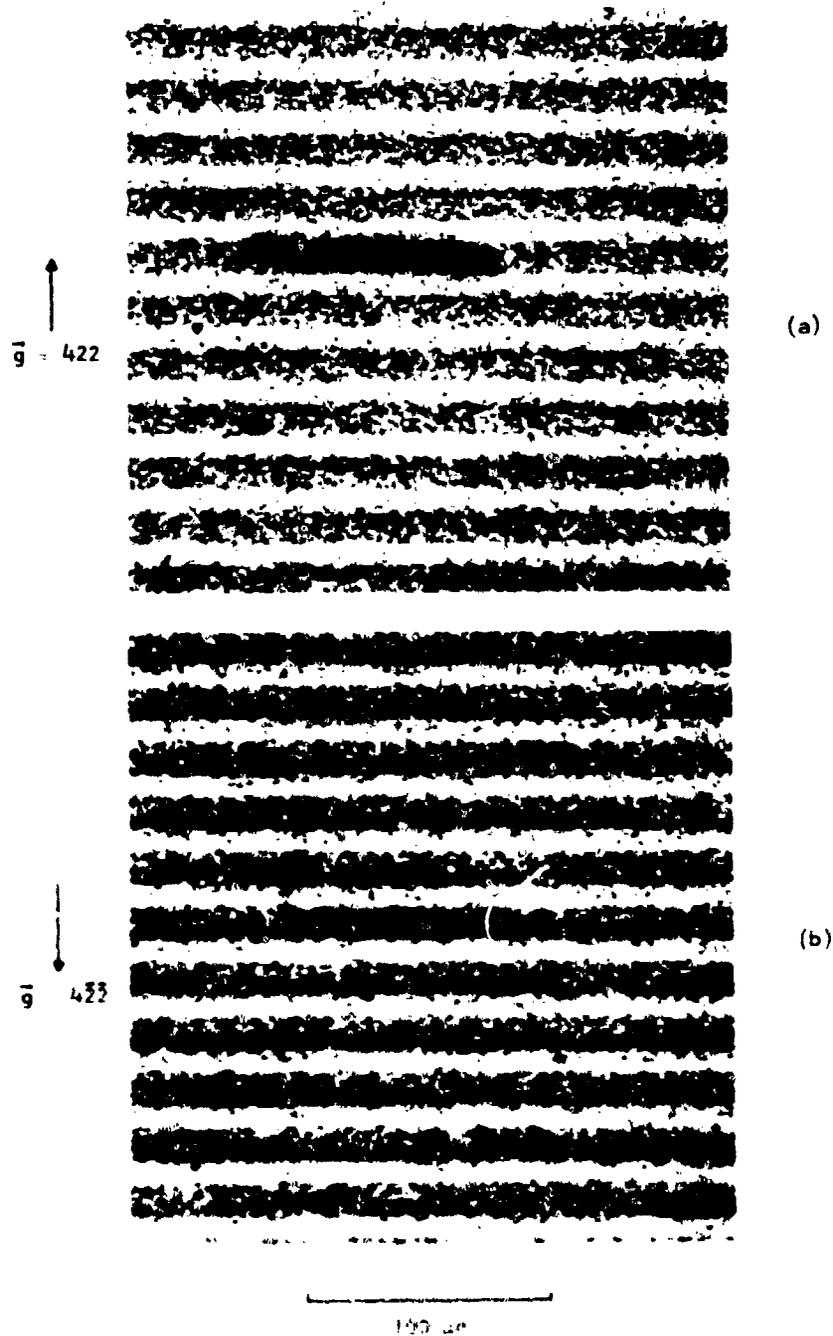
Figure 32 Electrically Inactive Dislocation in CCD Imager

$\vec{g} = 422$

100 µm
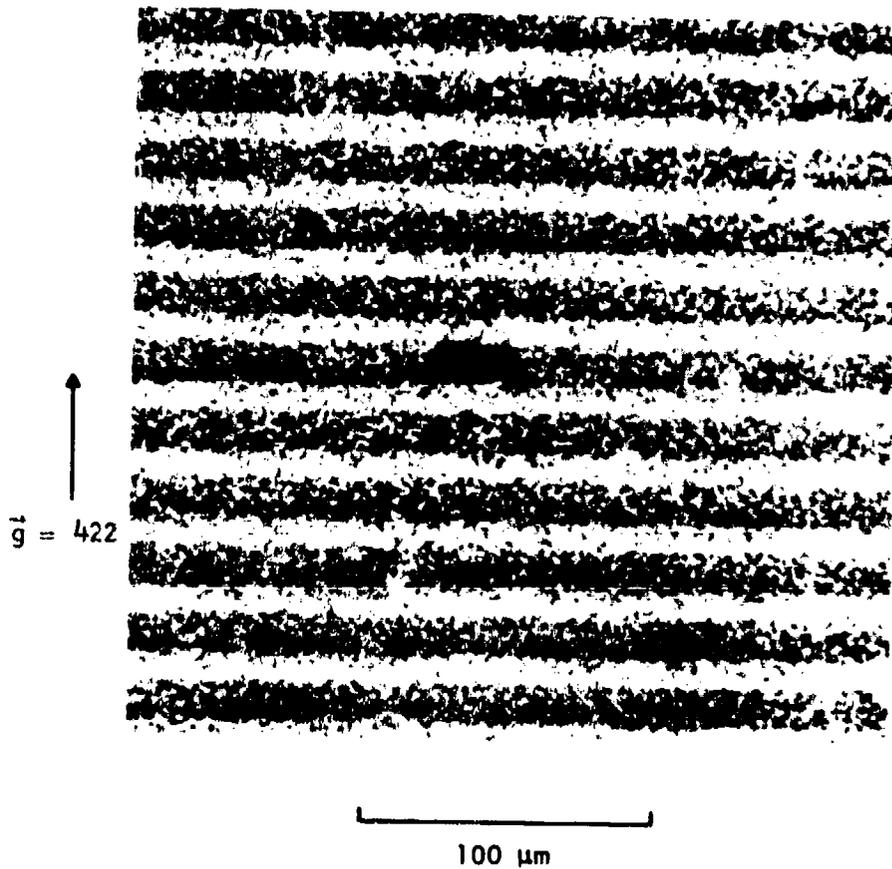
Figure 33 Electrically Inactive Dislocation in CCD Imager
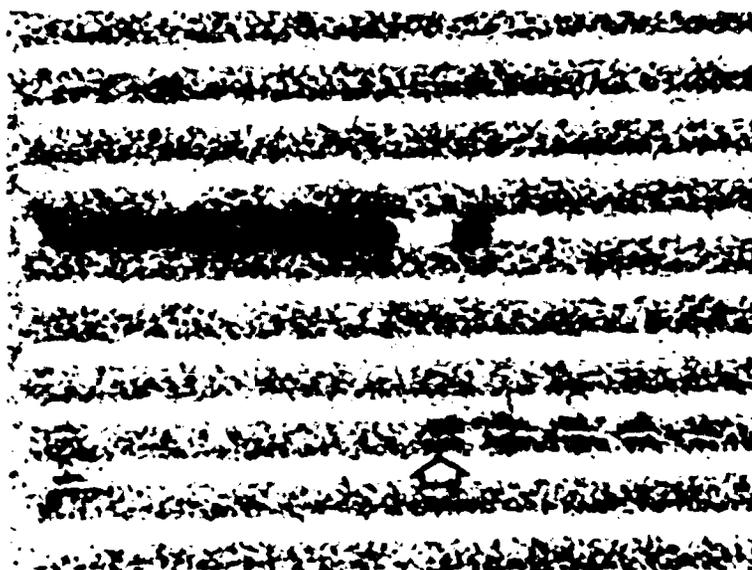
100 μm

Figure 34   Enlargement of Figure 30(a). Scratch (arrow) is on regions of a channel that were overlaid with polysilicon. Part of the disloca- tion has been pulled out of the channel stop by the overlying polysilicon.

63
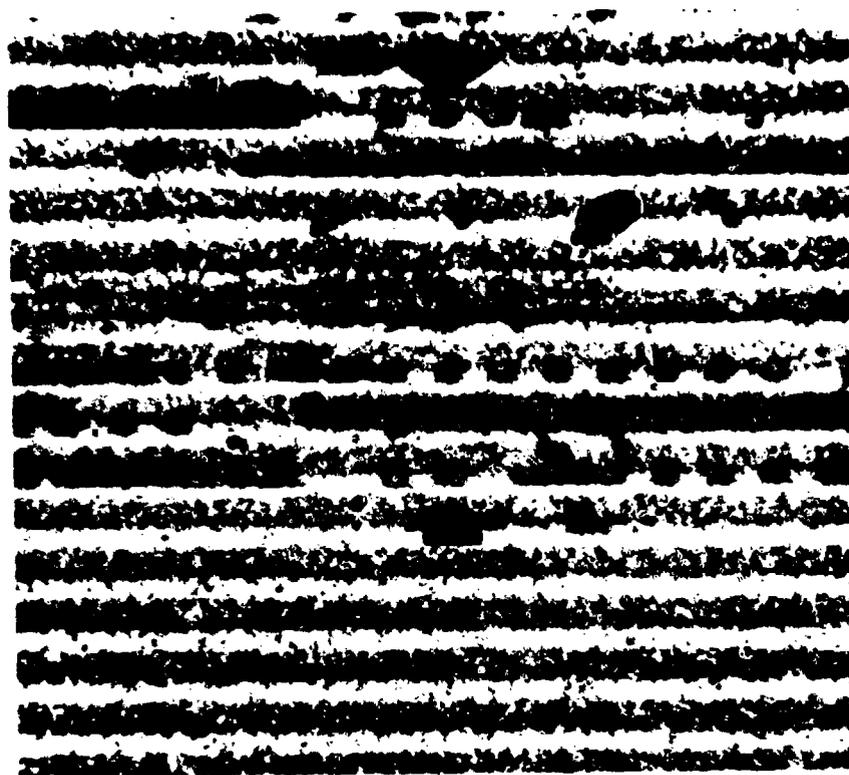
100 μm

Figure 35 Dislocation Segments in CCD Imager. The segments are approximately
12 μm long with a periodicity of 25 μm. Segments on different
channels/channel stops fall on a line perpendicular to the channels/
channel stops (arrows). Thus the segments are formed by action of
the polysilicon strain field on a continuous dislocation line.

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in this region, then it will produce dark current, with the current leaking over into the adjacent channel well.

The dislocations in Figures 32 and 33 are clearly in the depletion region of the device. Therefore, they must be electrically inactive. The origin of these dislocations is examined further in Section IV of this report.

An additional type of dislocation capable of producing dark current is shown in Figure 36. In this topograph only the tips of the dislocations are imaged, with the bulk of the loop penetrating to some depth (> 20 μm) into the silicon. Similar loops were found outside the array region of the device, in an area where the thick field oxide was grown. Their origin is obviously the thick oxide growth, but the formation mechanism is not clear. Contrast experiments showed they have a Burgers vector that is not in the plane of the surface, and their origin is probably through a slip process. The stress field of the thick oxide edge, however, is evidently not important in their formation.

Additional types of dislocations seen in some imagers, none of which have been observed to act as dark current sources, are shown in Figures 37 and 38. In Figure 37 the stess field of the polysilicon evidently assisted the nucleation and propagation of this dislocation, while in Figure 38, dislocation loops created during the swirl precipitation of oxygen served as the nucleation agents of these dislocations. Propagation is by the stress field of the thick oxide.

2.   Stacking Faults

Figure 39 is a reflection topograph of a portion of a device on which a scratch was placed before processing. The sources of dark current are indicated by the arrows in this figure.   It will be seen that the dark

65
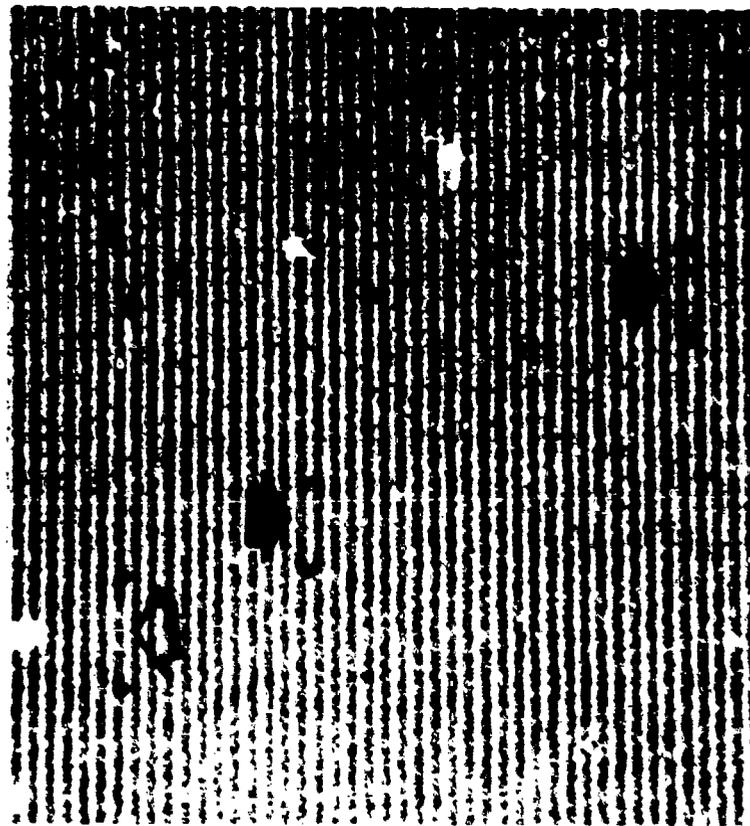
Figure 36   422 Reflection Topograph of Dislocation Loop in Channel Stops of
an Imager. Solid arrows indicate electrically active loops, open
arrow indicates a loop that is not a dark current source.
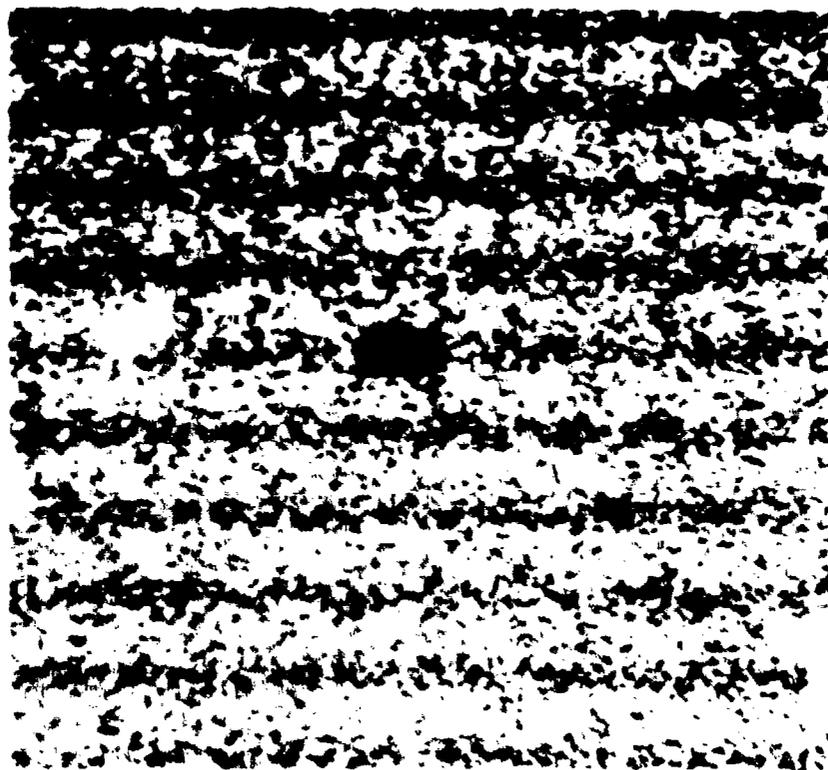
Figure 37 422 Reflection Topograph of Dislocation Segment Perpendicular to
Channels and Channel Stops. The dislocation extends from one
channel stop across a channel to the adjacent stop and is under-
neath the polysilicon electrode. It is not a dark current source.
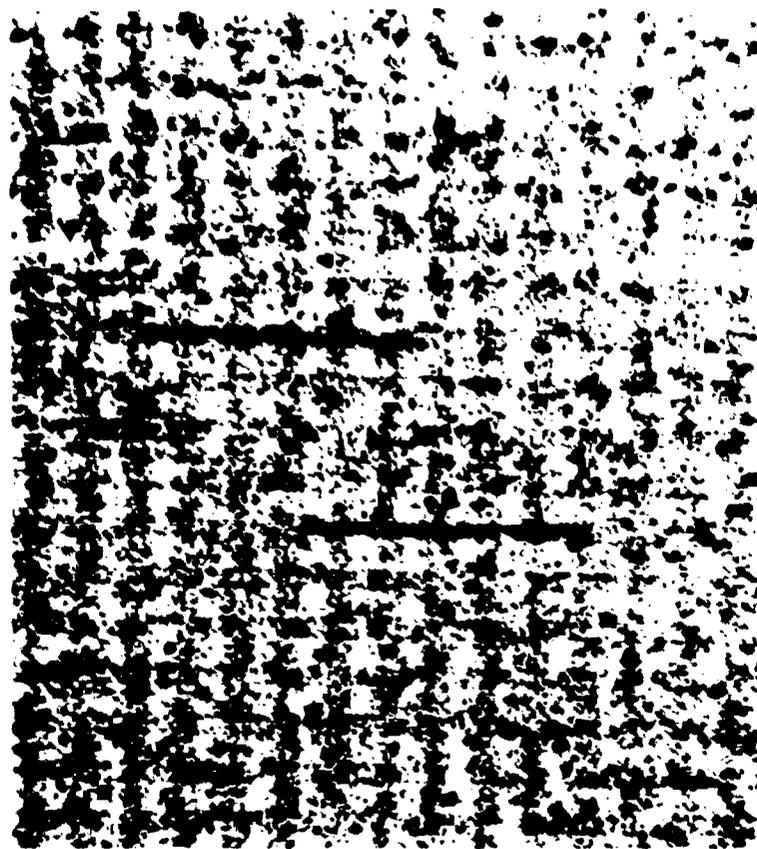
Figure 38 $42\bar{2}$ Reflection Topograph Showing Channel Stop Dislocations Nucleated from Subsurface Swirl Dislocation Loops
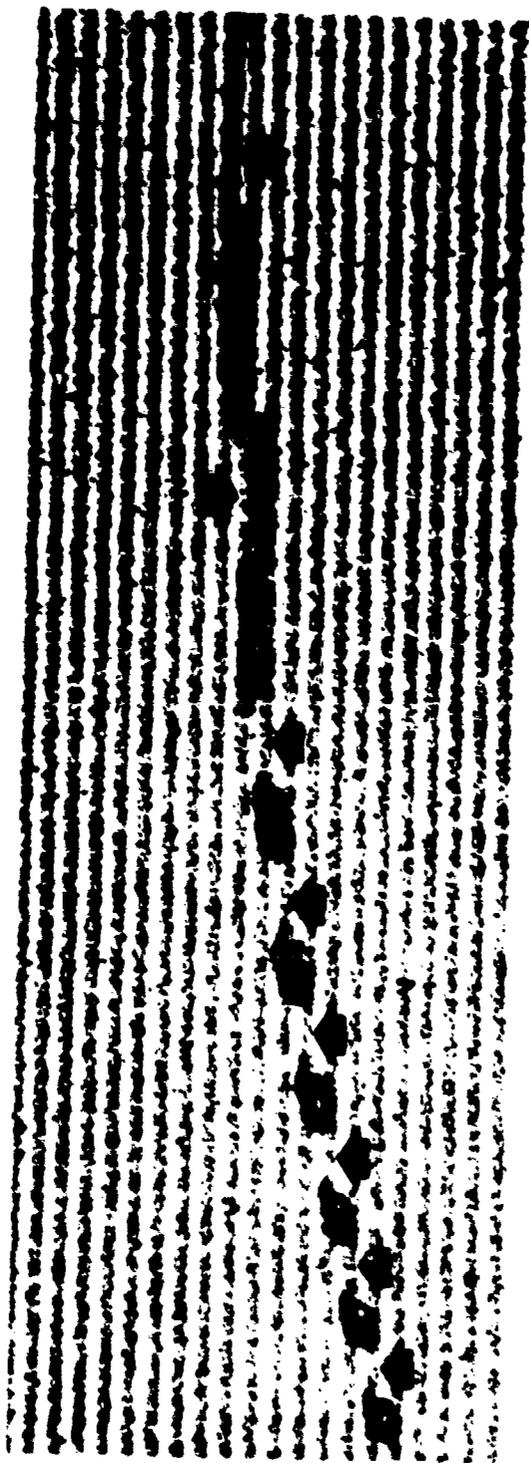
Figure 39 422 Reflection Topograph of Scratch on CCD Imager. Arrows indicate sources of dark current which occurred where scratch passed over a channel.

200 μm

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current originates where the scratches cross the channels (the channels appear dark in this figure). Since the defects produced by a scratch during oxidation are stacking faults and dislocations if unfaulting occurs, this figure clearly shows that stacking faults on the channel stop are not dark current sources, while stacking faults on the channel are dark current sources.

E.   Effect of Backside Damage on Defects in CCD Imagers

This subsection presents results of the experiments conducted by placing backside mechanical damage on half of a slice using sandblasting by 100 μm glass beads. The demarcation line between the damaged and undamaged halves of the slice was averaged so that there would be a line of CCD imagers down the slice which had part of their backsides damaged and part undamaged. The efficacy of the damage, therefore, was studied on the same slice and, as well, on the same imager.

The characterization consists of measuring the dark current for a 32 ms integration time and counting or estimating the number of dark current spikes per imager from the video display of the dark current. Devices are sorted into the arbitrary bins 0-20, 21-40, 41-100, 101-800, and > 800, according to the number of defects. The absolute numbers of devices in each bin are then converted to percentages to facilitate comparison between materials and between devices with and without backside damage.

*   Results

Devices from Group 2 had a high number of dark current spikes, relatively unaffected by the backside damage. However, some lowering of the total dark current as a result of backside damage was noted. The dark current readout of a device from this material category is shown in Figure 40. The upper third of the device has backside damage, the lower two-thirds none. Clearly, the density of dark current spikes is not altered dramatically by the

70
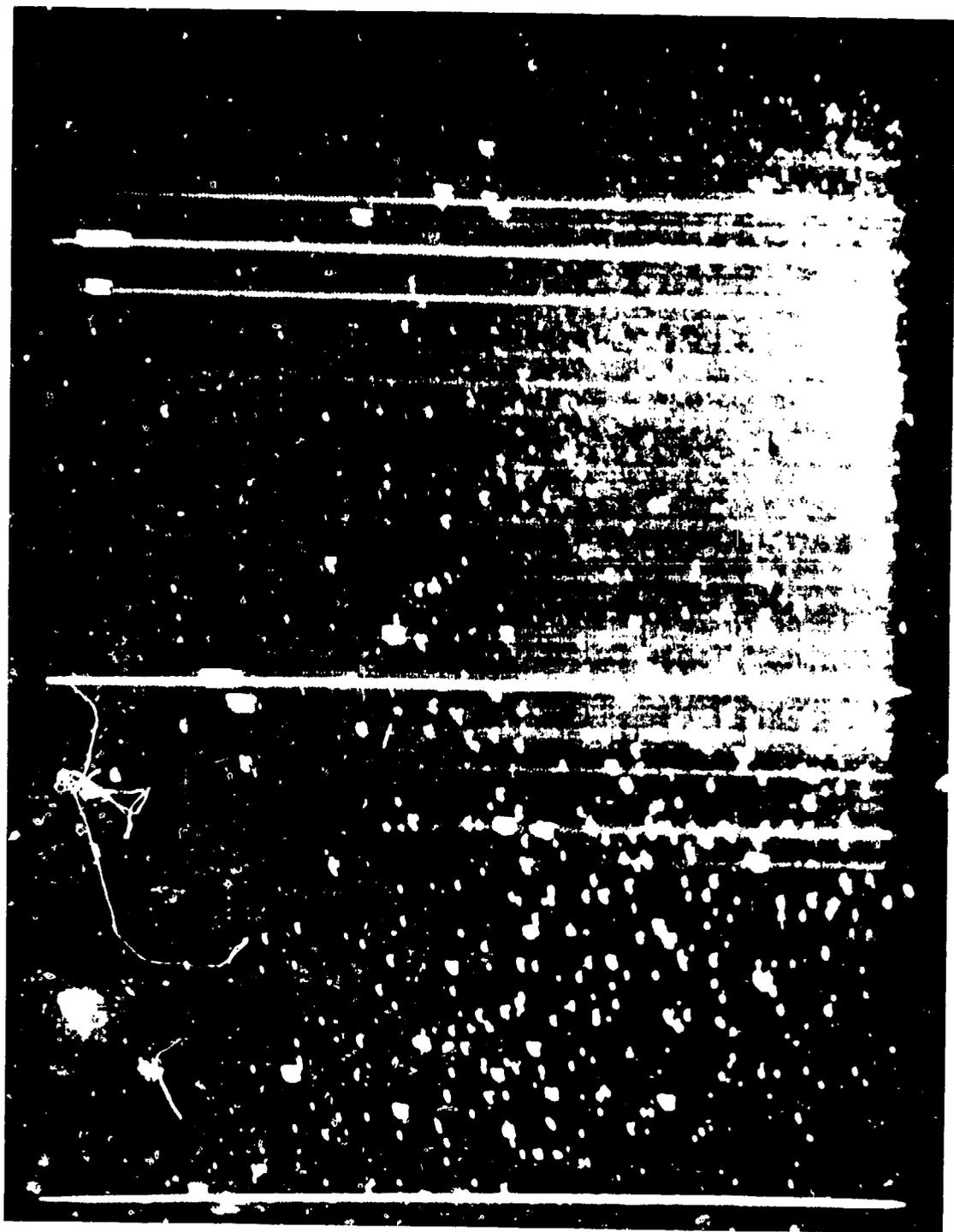
Figure 40 Dark Current Display of a CCD imager with 32 ms Integration Time. Backsid sandblast damage is on the upper third of the device.

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backside damage, although their intensity may be. Devices from several slices from Group 2 were characterized. As shown in Table 4, no meaningful dark current spike reduction was observed with backside damage. Some lowering of the background current, however, is indicated.

Slices from Group 1 were examined in the same way. The summary of device performance of several slices of this material, as given in Table 4, shows that a significant fraction of devices with backside damage have less than 100 dark current spikes, while all devices without backside damage have at least 100 defects per device. As before, some lowering of the background current is observed.

The imagers fabricated on Group 3 material have more than 100 dark current spikes per device. The same material with backside damage yields imagers with fewer dark current spikes. Most of the improvement is in bringing the defect count from the > 800 column to the 100 to 800 column. Examples of imagers on this material are given in Figure 41. Dark current photos are shown for two adjacent devices and for two different integration times (the time between CCD readouts). Only the bottom two-thirds of the lower device has backside damage. In addition, a significant decrease in the dark current occurs with the backside damage (Table 4).

While these results indicate that backside damage has a slightly beneficial effect, one control wafer in the lot showed degradation as a result of backside damage. This is illustrated in Figure 42. Here the dark current banding visible in devices without backside damage is replaced by dark current spikes on devices with backside damage. X-ray transmission topography, however, showed that this wafer received backside damage during processing similar to that which the float-zone slice received. As a result, dislocations were generated. The combination of the glass bead backside damage and process damage was sufficiently severe to cause dislocations to propagate to the front

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Table 4

Summary of Total Dark Current and Dark Current Backside Damage Tests

Material	Dark Current (nA/cm²)	Point Defect Distribution (%)				
		0-20	21-40	41-100	101-300	> 300
Group 2						
• With Backside Damage (BSD)	7.8	0	4	18	46	32
• Without BSD	12.0	0	0	13	47	40
Group 1						
• With BSD	7.1	7	20	7	46	20
• Without BSD	9.0	0	0	0	50	50
Group 3						
• With BSD	6.6	4	9	9	70	8
• Without BSD	11.2	0	5	0	33	62

32 msec

100 msec
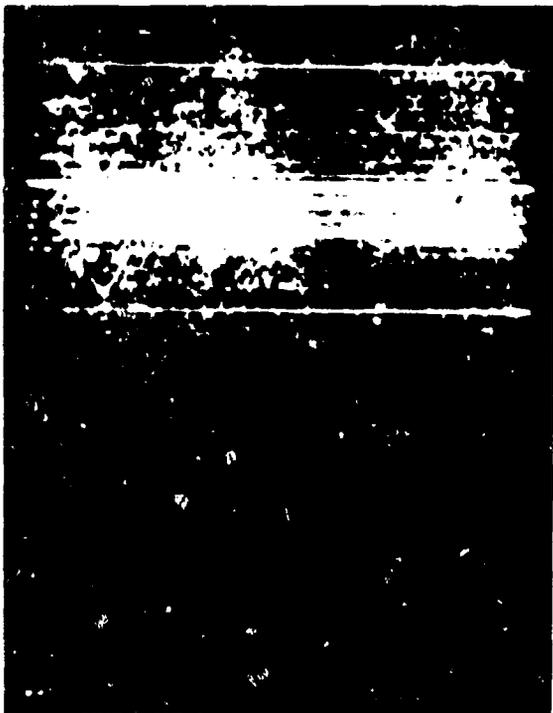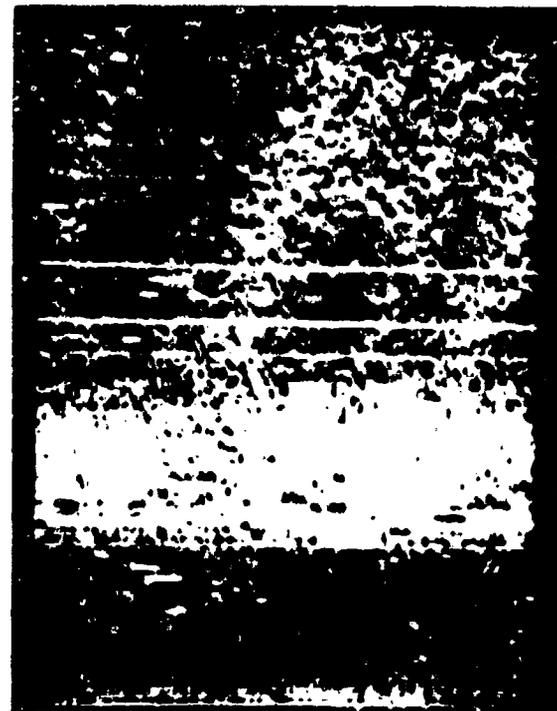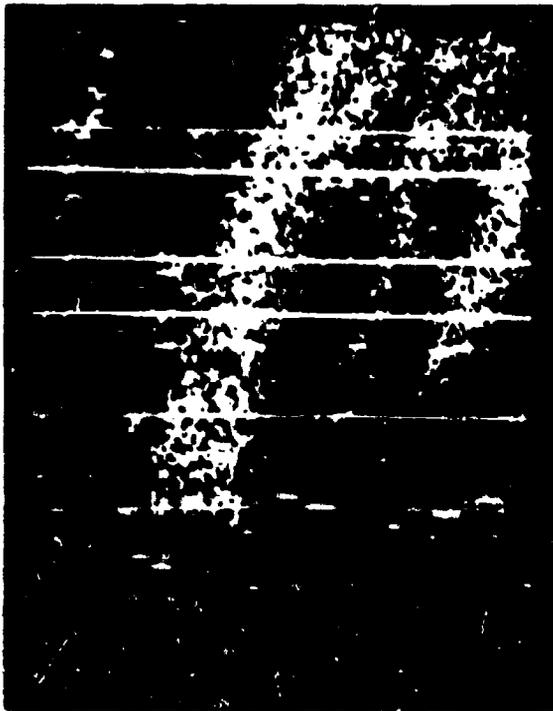
No
Backside
Damage

Backside
Damage

Figure 41   Dark Current Display of Two Adjacent Imagers for Integration Times of 32 ms and 100 ms. Backside damage was applied only to the lower two-thirds of the lower imager.

17.7 nA/cm^2

18.6 nA/cm^2

16.0 nA/cm^2

Backside Damage

No Backside Damage
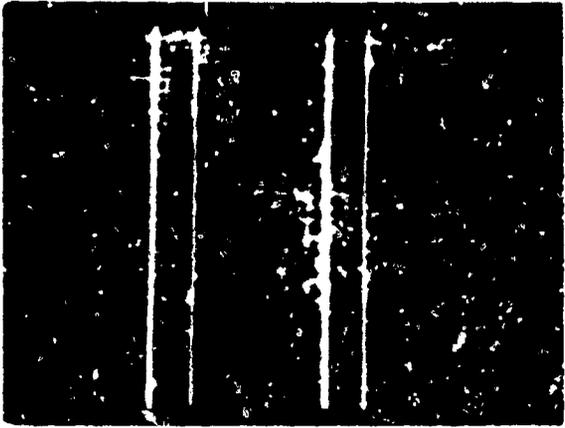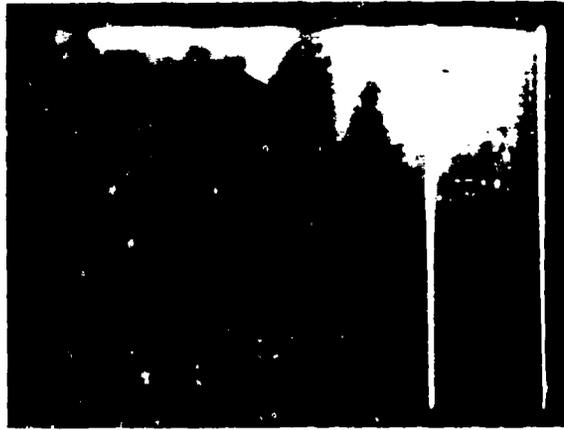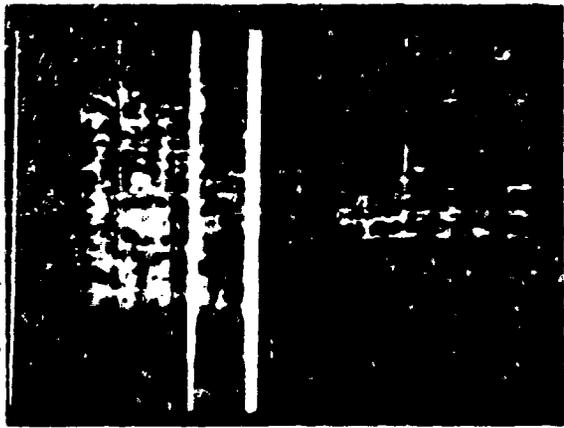
15.7 nA/cm^2

21.5 nA/cm^2

20.0 nA/cm^2
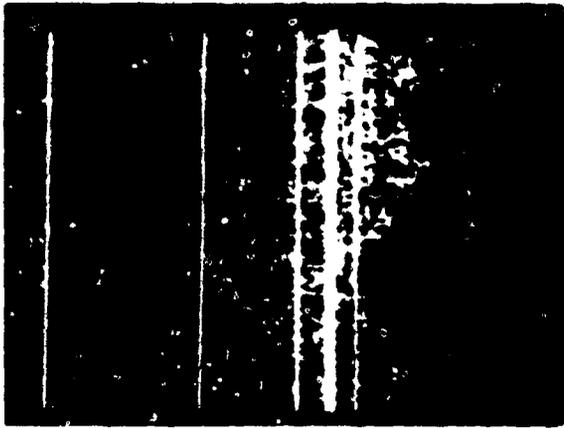
Figure 42 Dark Current Display, with Dark Current Readings, for Six Contiguous Devices. The lower left corner of the device with 21.5 nA/cm^2 is black because of readout failure in the device.

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surface where both were present. Thus, the dark current spikes are caused by dislocations. The mottled appearance of the dark current banding in the two center imagers of Figure 42 suggests that dislocations getter the dark current banding at close range. This is in agreement with previous observations.

F. **Results of ISS Backside Damage Tests**

Ten slices of material from Czochralski - Group 1 were treated with Impact Sound Stressing (ISS)[1] and returned to us for processing and evaluation. Five of these slices were matched with five untreated slices taken from neighboring positions in the boule and sent through the standard imager process.

X-ray transmission topographs were taken of the finished slices (Figure 43). This superposition of device geometry with the damage pattern reveals that there are six devices at the slice center where the damage pattern is uniform across the whole device. At first sight, it would seem that one way to judge the effectiveness of ISS would be to compare the quality of these six devices with that of devices on the same slice that come from the outer, undamaged part. Such a comparison is invalid, however, because the slices that were not ISS-treated do not display a uniform density of dark current spikes. Rather, the efficacy of ISS must be judged by a comparison of the center six devices on ISS-treated material with those on untreated material.

Typical results for the untreated control slices are shown in Figure 44. Here, two adjacent devices from two slices illustrate the range of dark current spikes found on the center six devices. Typical devices from the ISS-treated slices are shown in Figure 45. From these results, we conclude that the ISS treatment does not lead to significant improvement in the density of dark current spikes on this material.
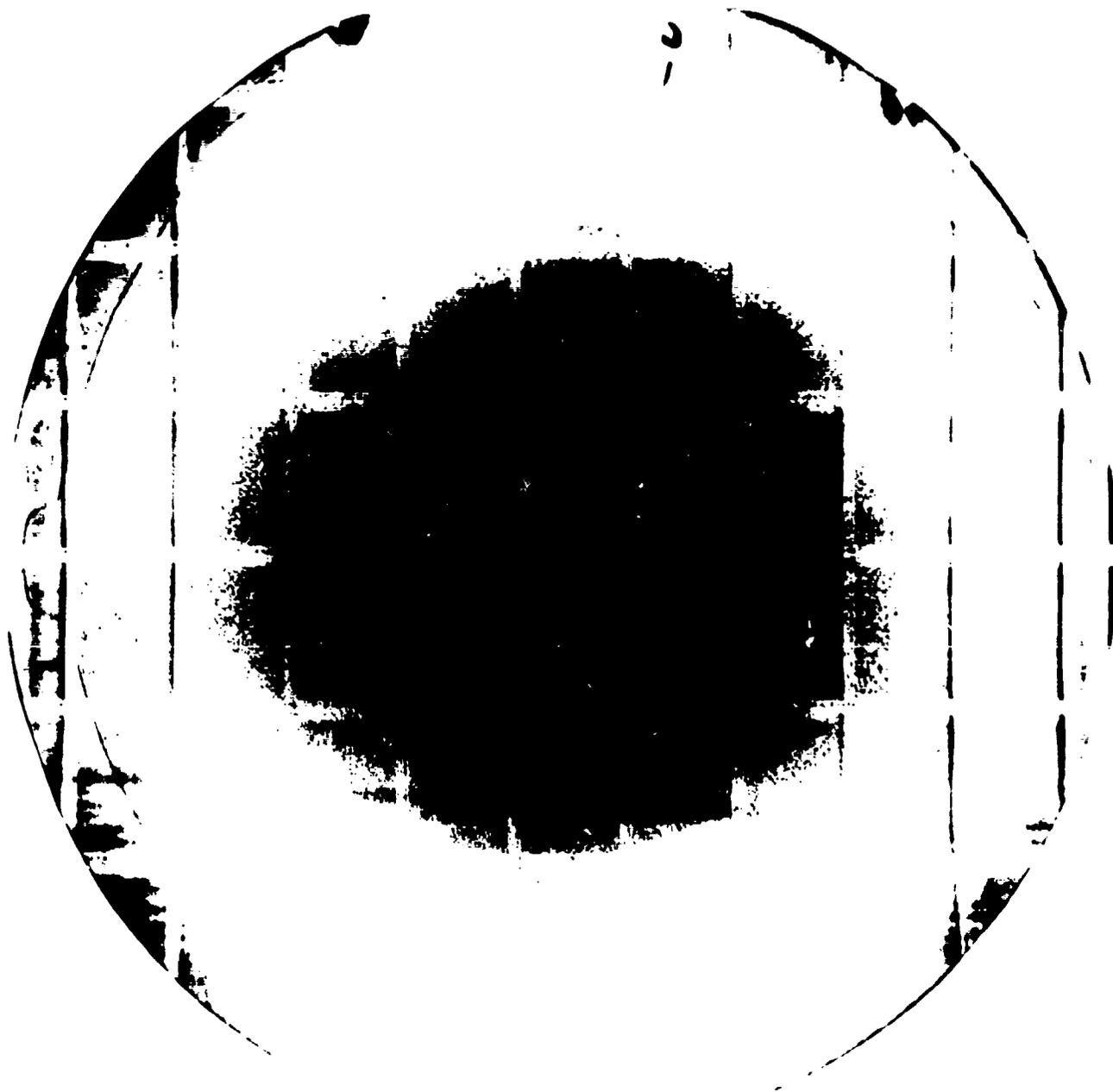
Figure 43 (220) Transmission Topograph Showing Pattern of ISS Backside Damage
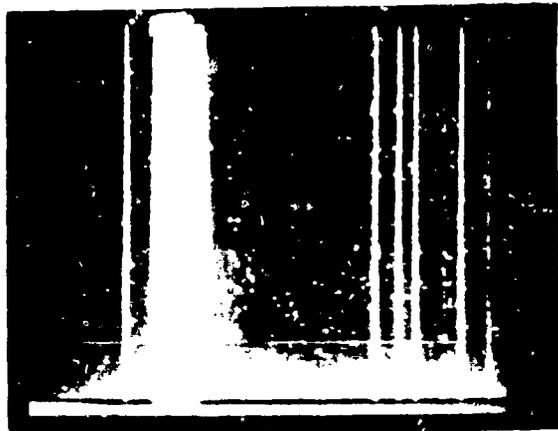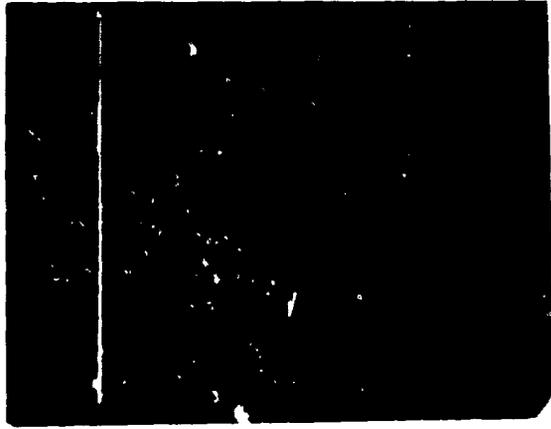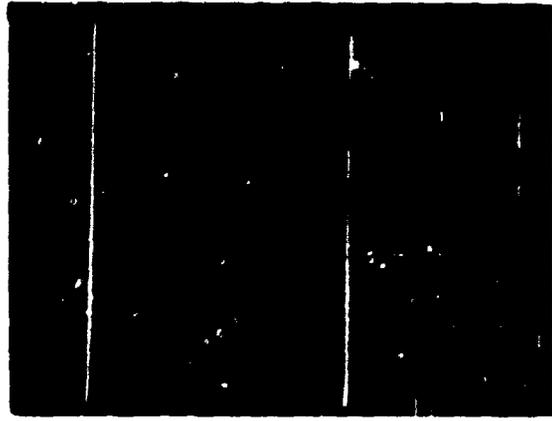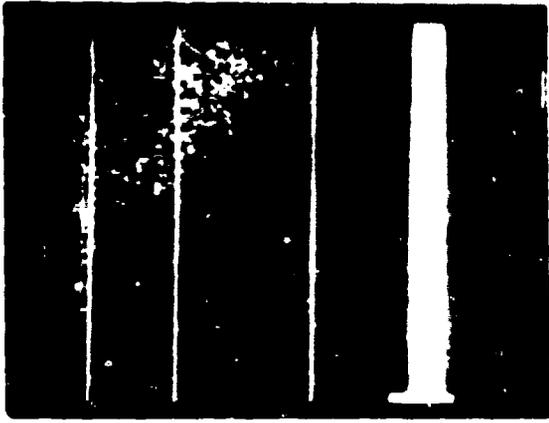
Figure 44 Dark Current Readout of Typical Devices on Control Slices Not Treated with ISS

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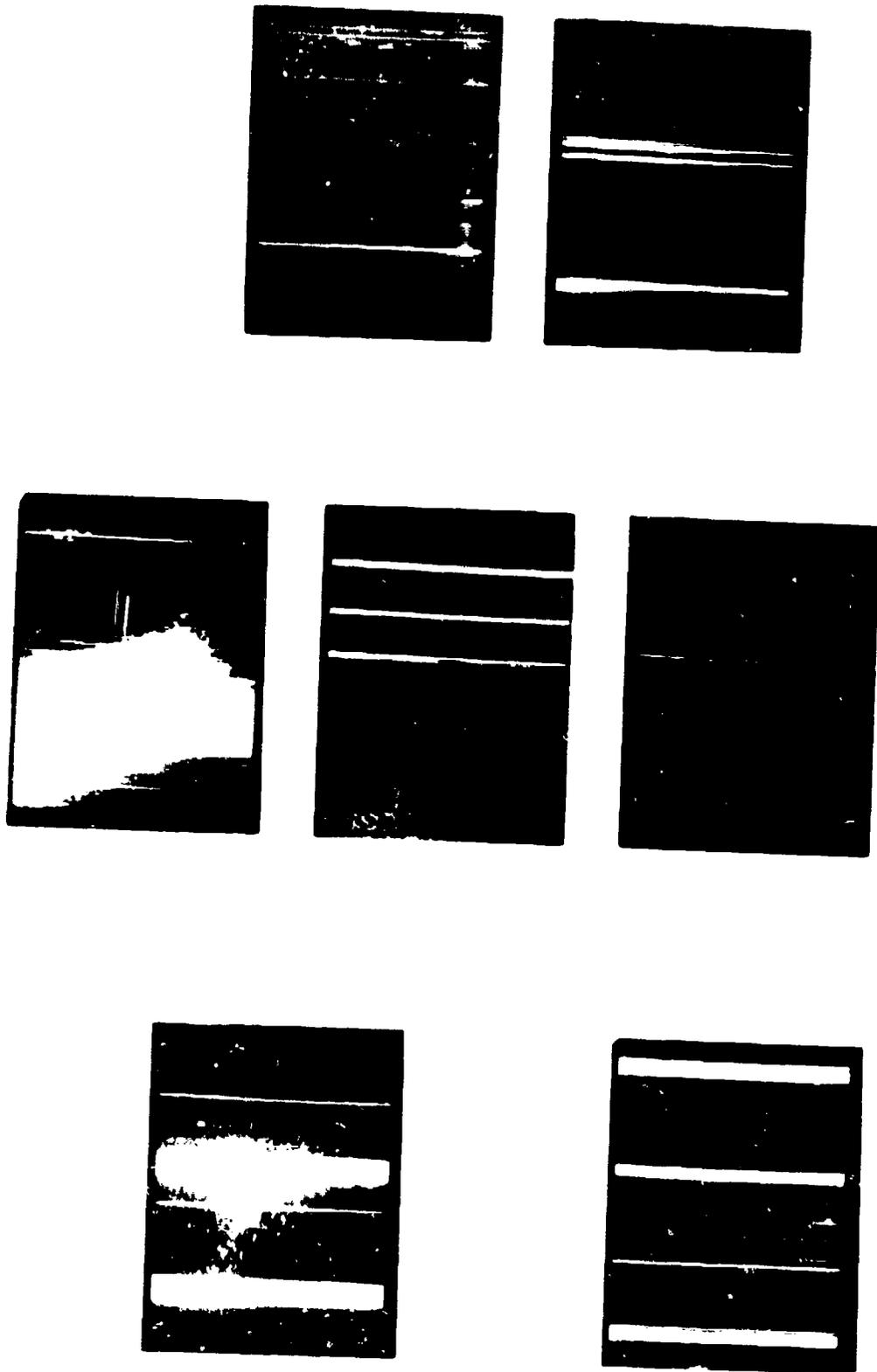
Figure 45   Dark Current Readout of Typical Devices from Slices Treated with the
ISS Backside Damage

It should be noted, however, that the processing of these slices included gettering steps as a standard feature. A second set of five slices with the gettering steps eliminated encountered processing problems, and no devices were operational. It does not seem likely, however, that these steps would counteract the effectiveness of the ISS treatment. In addition, ISS-treated slices of material from Czochralski - Group 3 (where the effect of glass bead backside damage showed positive results) and from the float-zoned group are being processed without these process gettering steps, but have not been completed at this writing.

SECTION IV
IN-PROCESS X-RAY TOPOGRAPHY

A.   Introduction

To determine at what point in the process defects originate, in-process x-ray topographic studies were made. A series of slices was selected from each of the groups of materials and committed to processing. X-ray topographs were taken after each high temperature processing step. Because of the extreme sensitivity of reflection topographs to the stresses produced by the device overstructure, it was decided to use transmission x-ray topography as the chief investigative tool. Here, we would make use of one of the chief advantages of x-ray topography: its nondestructive nature. Unfortunately, because of the small size of most defects, as outlined in Section III.B, the only defects that were imaged were dislocations and bulk swirl precipitation. Furthermore, because of processing problems, probably caused by the extensive handling and additional cleanups the slices received, very few of the imagers were operational. Nevertheless, the results of the in-process studies clearly show the origin and development of the channel and channel stop dislocations.

B.   Results

Figure 46 is a series of topographs of a region of an imager taken after various high temperature processing steps. In Figure 46(a) no channel/channel stop dislocations are apparent after the channel stop (boron) deposition. After boron drive/thick oxide growth, there are channel/channel stop dislocations [Figure 46(b)]. Furthermore, during phosphorus deposition and drive, in which the array portion of the device sees only an anneal, two of the dislocations grow [arrows, Figure 46(c)].

Figure 47 is a high resolution transmission topograph of a portion of this same array taken under different diffraction conditions after thick oxide growth/boron drive. This topograph shows that the dislocations are nucleated

81

(a)

(b)

$\bar{g}$ 220
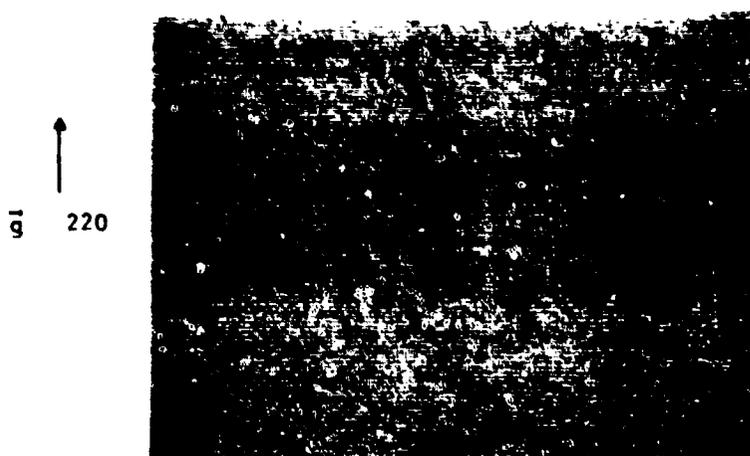
(c)

Figure 46   Transmission Topographs of CCD Array After Various Processing
Steps.   (a) After boron deposition, (b) after boron drive/thick
oxide growth, (c) after phosphorus deposition/drive.   Arrows in
Figure 46(c) indicate dislocations that have grown.

$\vec{g} = 2\bar{2}0$ →
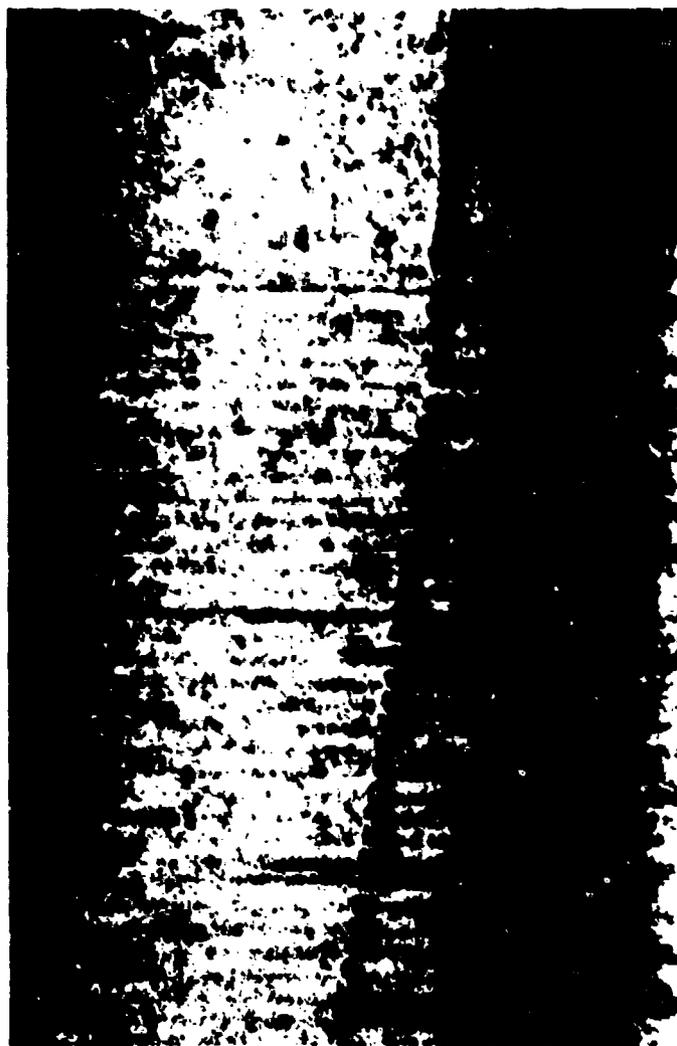
|—— 100 μm ——|

Figure 47 Transmission Topograph of Array Showing Nucleation of Channel/Channel
Stop Dislocations From Scratch. After boron drive/thick oxide growth.

from a scratch. Furthermore, the scratch is imaged as a pair of lines outside the array in a region that has been subjected to thick oxide growth. In the array the scratch appears as a serrated image because defects develop on the scratch only during oxidation cycles, which for the array are primarily on the channel stops during thick oxide growth.

The thick oxide produces a stress in the silicon which is a maximum at the thick oxide edge, i.e., at the channel stop/channel interface. The stress arises from the differences in the coefficients of thermal expansion of the oxide and silicon. It is at this high stress region that dislocations are generated, as may be seen in Figure 48, if a nucleation site of sufficient intensity is provided. In Figure 48, scratches that have been subjected to thick oxide growth are present where dislocations are generated.

We are thus led to following scenario for the formation of channel stop/channel dislocations. A nucleation site must be present near the channel stop/channel interface. This nucleation site may be a dislocation, a scratch of sufficient intensity which has been subjected to thick oxide growth, or some as-yet unidentified defect in the starting material. After thick oxide growth, and probably during cooling of the wafer, the dislocations are formed due to stress concentration formed at the edge of the thick oxide. This stress is insufficient to generate a dislocation in the perfect silicon, but is sufficient to generate a dislocation if a proper nucleating site is present. The dislocations are then propagated by the stress field of the thick oxide edge. Whether they fall on channels or channel stops will depend on the Burgers vector of the dislocation generated, and hence its interaction with the thick oxide stress field. During subsequent heat treatments, the dislocations may propagate further, but we find no evidence for the generation of new dislocations from existing or newly activated nucleation sites.

84
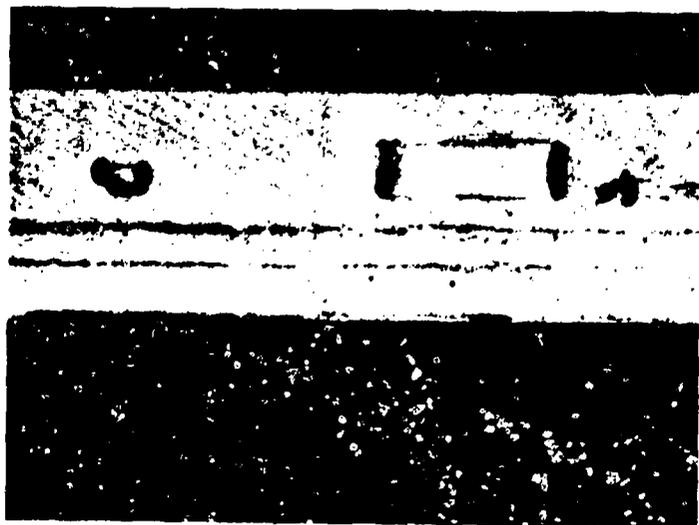
$$\vec{g} = 220$$

Figure 48 Transmission Topograph of Device Edge Showing
Nucleation of Dislocations at Scribe Line
Edge

The surface of one of the slices was intentionally scratched in a spiral pattern with silicon carbide grit to follow the evolution of stacking faults during processing. A transmission x-ray topograph of this wafer before the beginning of processing is shown in Figure 49. Immediately after the initial oxidation, the intensity of the contrast from the scratch is significantly reduced (Figure 50). This contrast results from the removal of the strain centers left by the scratching medium, and the complete conversion of the scratch to stacking faults.[13,14]

Subsequent processing shows that the scratch continues to undergo changes. Figure 51 is a series of topographs of the same region of a test bar after certain processing steps. After boron deposition, but before boron drive/thick oxide [Figure 51(a)], the intensity of the scratch damage is significantly reduced in regions that have been opened for boron deposition. After thick oxide growth [Figure 51(b)] the contrast from scratches in this area reappears, while the contrast in regions that have been masked off from oxidation subsides. At this point, dislocations at the edge of the thick oxide region also appear. Finally, after phosphorus diffusion and drive [Figure 51(c)], the scratches reappear in the regions that had not undergone thick oxidation. Additional dislocations are produced at oxide boundaries that are opened prior to phosphorus deposition.

As expected, defects produced from scratches were found to be dark current sources.[15] Figure 52(a) is a dark current map of an operational device on this slice. Figure 52(b) is a transmission topograph at the completion of processing of this same device. There is an exact correlation between the scratches and the dark current in this device.

A sample for transmission electron microscopy was taken from the lower left-hand corner of the device. It was found that the defects present in this region consisted of stacking faults and dislocations from unfaulted stacking
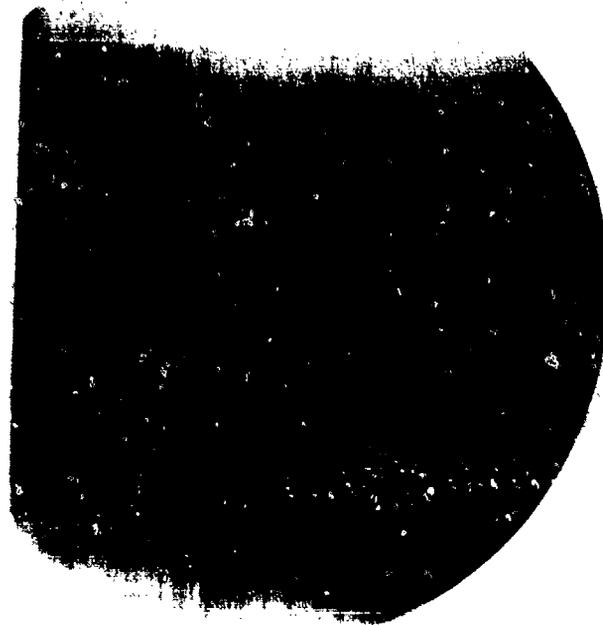
1 cm

Figure 49   Transmission X-Ray Topograph of Intentionally Scratched Slice Before
Initial Oxidation
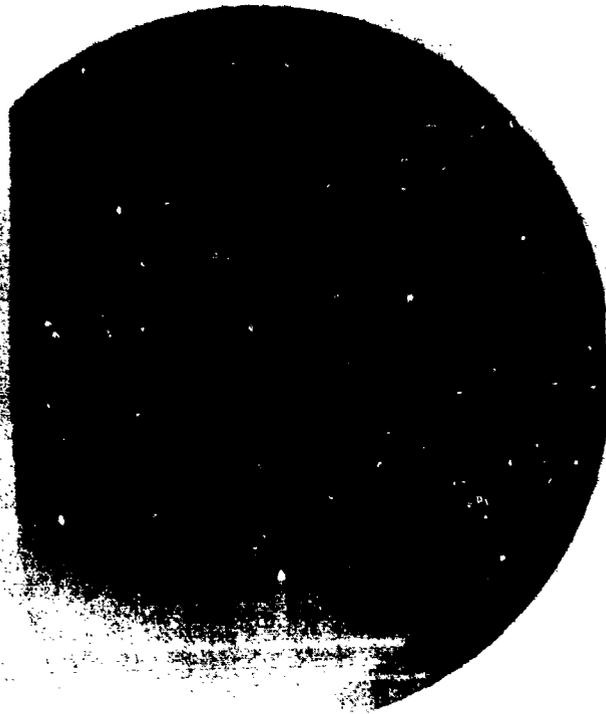
1 cm

Figure 50 Transmission Topograph of Intentionally Scratched Slice After
Initial Oxidation

$\vec{g} = 220$
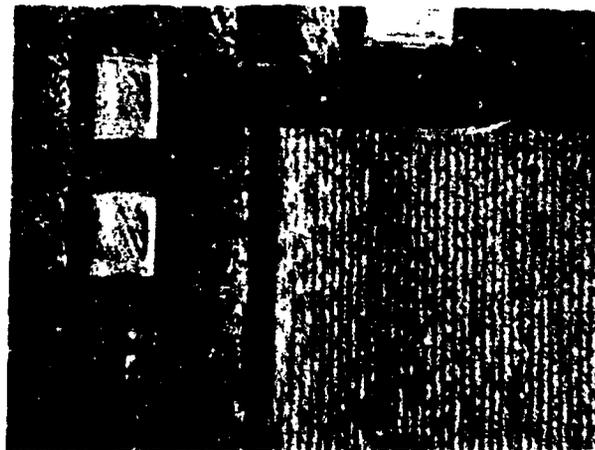
Figure 51   Transmission Topographs of Test Bar After Various Process Steps.
(a) After boron deposition, (b) after boron drive/thick oxide
growth, (c) after phosphorus deposition/drive.

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(a)   (b)

Figure 52 Dark Current Produced by Intentional Preprocess Scratch. (a) Dark current map, (b) transmission x-ray topograph.

faults. Typical stacking faults are shown in Figures 53 and 54. Stacking faults in the channel were of two types: those near the center were consistently 1 to 1.3 μm long, while those near the edge of the channel were somewhat longer and deeper, up to 7.5 μm in length. Most of the stacking faults in the channel were underneath polysilicon. Stacking faults that crossed the boundary were intermediate in length. Dislocations from unfaulted stacking faults were seen only in regions where high density of stacking faults was present.

An interesting feature of the stacking faults that crossed the boundary is that many of them show signs of shrinkage (Figure 55). In Figure 55, the curvature of the bounding Frank partial is different from that which we have seen on any other stacking fault, in that it is curved into the stacking fault near the surface rather than away from the stacking fault. Such a curvature could occur if the stacking fault were shrinking by a bulk diffusion mechanism. Here, the stacking fault dissolves by the emission of silicon interstitials from the Frank partial into the bulk. This causes the Frank partial to climb toward the surface. These interstitials diffuse away through the bulk. The curvature at the surface would occur because the surface is incapable of sinking interstitials and therefore acts as a mirror to the interstitials, reflecting them back into the solid. Under this latter situation, the solid angle into which the shallow Frank partial could emit interstitials is half the solid angle into which the Frank partial lying deeper in the bulk could emit interstitials: hence, the deeper-lying Frank partial will climb at twice the rate of the shallower Frank partial. The operation of the climb-annihilation mechanism helps explain the shallow dislocations resulting from the unfaulting reaction found in other devices.

The observations reported here clearly show that during an oxidation process, stacking faults grow, while during a nonoxidizing high temperature process, the stacking faults shrink. Evidently, the shrinkage process may occur by two mechanisms. (1) In the presence of a thermal oxide, the stacking

(a)

i μm

(b)

1 μm
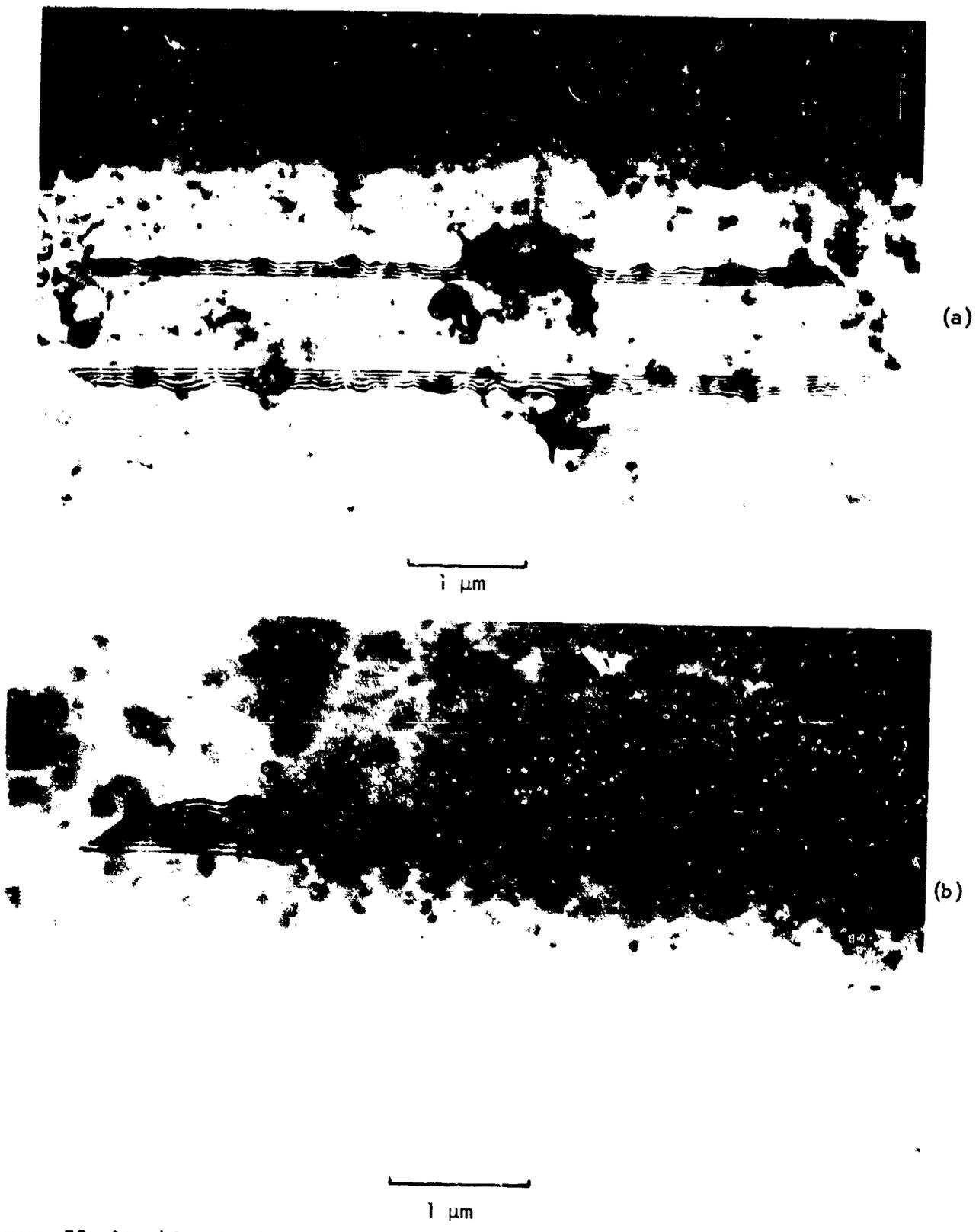
Figure 53 Stacking Faults in Imager Nucleated from Intentional Scratch. (a) In
channel stop, (b) in channel at edge of channel stop.

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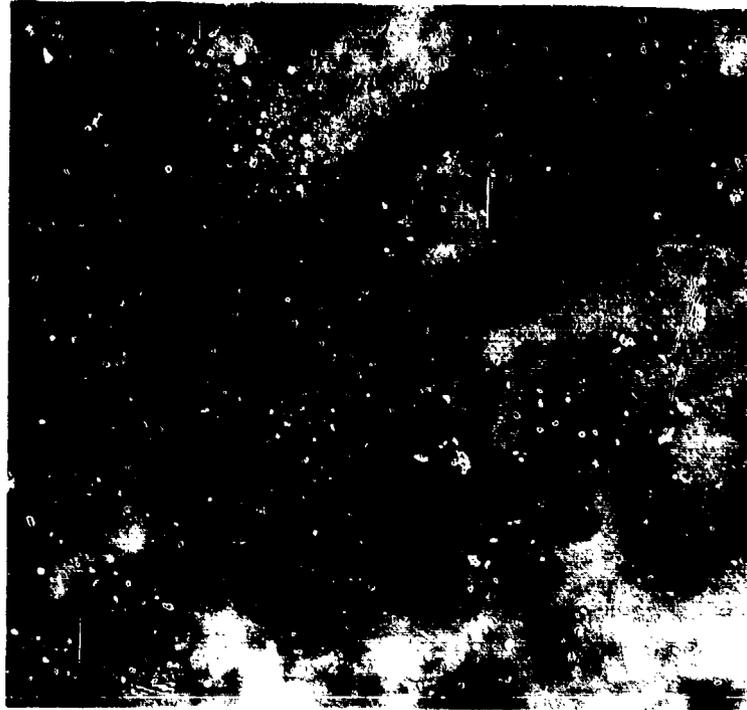
0.5 μm

Figure 54 Stacking Faults in Center of Channel Nucleated from Intentional
Scratch

0.5 μm
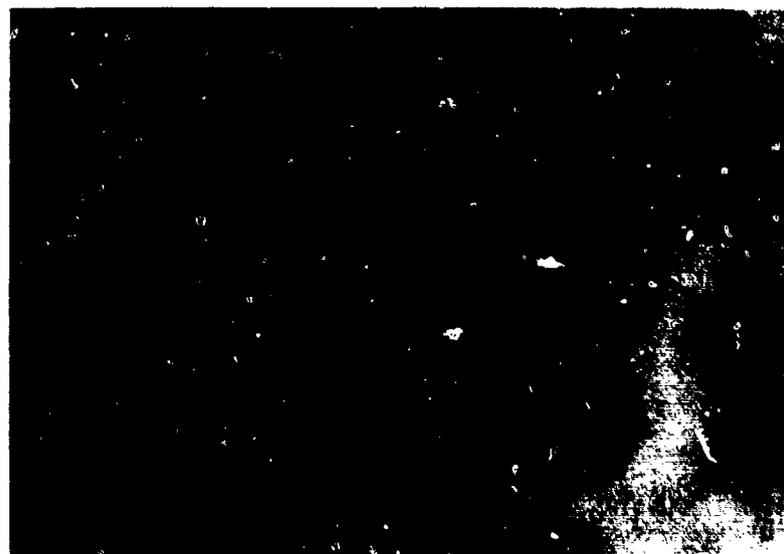
Figure 55 Shrinking Stacking Fault. Note reverse curvature of Frank partial at arrow.

faults shrink by the bulk diffusion of silicon interstitials away from the Frank partial, with the oxide interface reflecting the interstitials back into the bulk. Some recent measurements on the shrinkage of stacking faults underneath a thermal oxide show an activation energy similar to that of the self-diffusion coefficient of silicon.[16] In the absence of a thermal oxide, Sanders and Dobson showed that stacking faults shrink at a much greater rate under nonoxidizing heat treatment, and with a much lower activation energy.[9] Evidently, in the absence of a thermal oxide, the silicon surface can act as a sink for interstitials, and shrinkage then progresses by pipe diffusion of interstitials along the Frank partial to the surface.

It is interesting to note that Hashimoto, et al.[16] recently reported that stacking faults shrank with an activation energy similar to that observed by Sanders and Dobson[9] when boron and arsenic were driven underneath a chemically deposited oxide. They interpreted this as a "gettering" by the impurity. In line with our previous argument, it seems much more likely that a deposited oxide allows the surface to act as a sink for interstitials, and hence allows pipe diffusion. In this respect, a chemically deposited oxide may be inherently different from a thermal oxide. This suggests ways to minimize the occurrence of defects, as we shall propose in the last section of this report.

In the light of the foregoing discussion, we may understand the changes in the topographic contrast observed in Figure 51. During boron deposition, which is a nonoxidizing high temperature operation, stacking faults underneath the oxide shrink, but at a very low rate. Where the oxide has been removed and a free silicon surface exists, the stacking faults shrink, but at a very much more rapid rate. This is not a consequence of the presence of the boron impurity, but results because the thermal oxide has been removed in this region, and the surface can then act as a sink for interstitials. Evidently, this short heat treatment is not sufficient to totally eliminate the stacking

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faults, for in the subsequent oxidation, the stacking faults grow. However, during this oxidation, stacking faults lying under the oxide/nitride shrink by the bulk diffusion mechanism, since no oxidation is taking place in these regions. Again, the stacking faults are not totally eliminated, but grow during a subsequent oxidation step, this time also producing dislocations at oxide windows due to unfaulting.

SECTION V
UNFAULTING OF STACKING FAULTS IN SILICON

A. Introduction

It is well established that extrinsic stacking faults are produced from surface scratches when a silicon wafer is oxidized.[13,14] After prolonged oxidation, or after multiple oxidation cycles, dislocations in a predominantly pure edge configuration also are seen.[14] It has been concluded that these dislocations arise from the unfaulting of stacking faults.[17] In this section we report on observations of the unfaulting reaction in process.

B. Experimental

Wafers of (001) p-type Czochralski-grown silicon, 8 to 15 Ω-cm, were surface abraded using 6 μm diamond paste, or by using a wet cotton swab dipped in 300 grit SiC powder. After thorough cleaning, the wafers were subjected to a variety of steam oxidations ranging from single oxidations of four hours at 900°C to four hours at 1100°C, and multiple oxidation cycles at 1050°C. In many cases, the wafers were essentially air-quenched by a rapid pull from the oxidation furnace in two seconds or less. The surface oxide was then removed, and specimens were thinned for observation in the transmission electron microscope. Most of the observations were performed on a Siemens IA microscope operating at 125 kV. Weak-beam observations and x-ray analyses were made on a JEOL-1000X microscope equipped with a field emission gun and STEM attachment and operating at 100 kV.

C. Results

In all samples examined, the predominant defects were found to be stacking faults bounded by Frank partial dislo   ions and dislocations with Burgers vectors in the plane of the surface (001) of the wafer and in a predominantly edge orientation. The size of the stacking faults ranged from

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less than 1 μm to > 10 μm, with intersecting arrays of stacking faults frequently found.

In samples that had been subjected to a rapid pull, a small fraction (≤ 1%) of the stacking faults were found to be in the process of unfaulting. An example of a nearly completely annihilated stacking fault is shown in Figure 56. The assignment in Figure 56(c) is made on the following basis: There are three possible reactions by which a perfect dislocation will produce two partial dislocations separated by a stacking fault:

$$(1) \quad 1/2\langle \bar{1}\bar{1}0 \rangle \rightarrow 1/6\langle \bar{1}\bar{1}2 \rangle + 1/3\langle \bar{1}11 \rangle; \text{ stacking fault on (111)} \quad (1)$$

$$(2) \quad 1/2\langle \bar{1}\bar{1}0 \rangle \rightarrow 1/6\langle \bar{2}\bar{1}1 \rangle + 1/6\langle \bar{1}2\bar{1} \rangle; \text{ stacking fault on } (1\bar{1}1) \quad (2)$$

$$(3) \quad 1/2\langle \bar{1}\bar{1}0 \rangle \rightarrow 1/6\langle 2\bar{1}\bar{1} \rangle + 1/6\langle \bar{1}2\bar{1} \rangle; \text{ stacking fault on } (1\bar{1}\bar{1}) \quad (3)$$
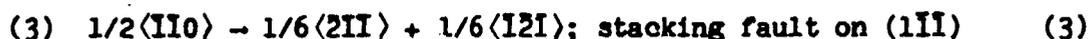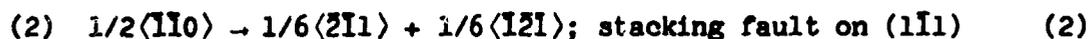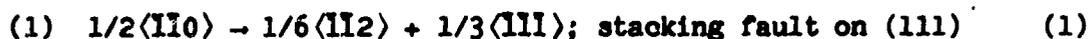
Imaged in the TEM under two-beam conditions with $\vec{g}$ = 220, the partial dislocations in reaction (1) would be visible along with the stacking fault; for reactions (2) and (3), the partial dislocations would be visible, but the stacking fault would be out of contrast. When $\vec{g}$ = 2$\bar{2}$0, the Shockley partial and stacking fault of reaction (1) would be invisible, while the Frank partial would show weak contrast where it did not lie in a $\langle 1\bar{1}0 \rangle$ direction. The partial dislocations of reactions (2) and (3) would be out of contrast for this reflection, but the stacking fault would be in contrast. Clearly, reaction (1) is the only case consistent with Figures 56(a) and 56(b).

Examination of Figure 56 shows that the perfect dislocation created by the unfaulting reaction has moved off the (111) plane on which it was created (we shall show below that the stacking fault is, in fact, being annihilated rather than created), illustrating that some time has elapsed since the unfaulting has occurred. Note also that the Shockley partial is curved into the stacking fault.

Figure 57 illustrates a freshly unfaulted stacking fault. In this figure a perfect dislocation (out of contrast) has dissociated on the stacking fault

98

(a)

g = $\overline{2}\overline{2}0$

(b)

g = $\overline{2}\overline{2}0$

(c)

δD

$C\delta$

CD

0.1 μm
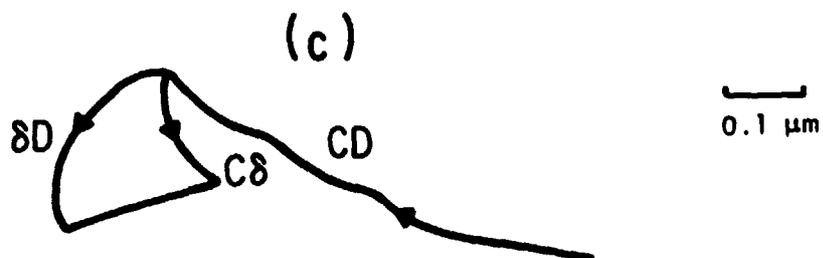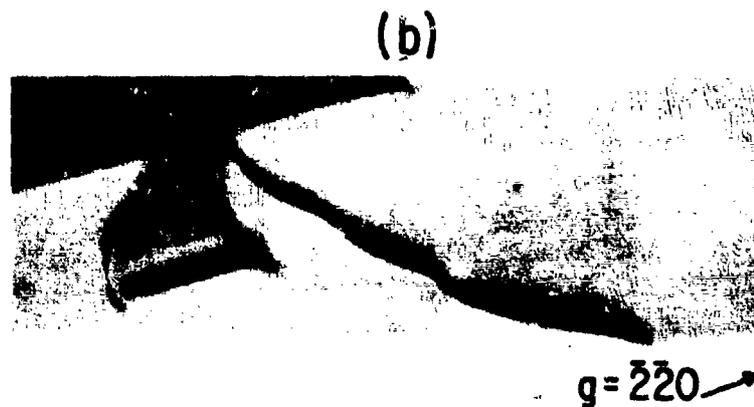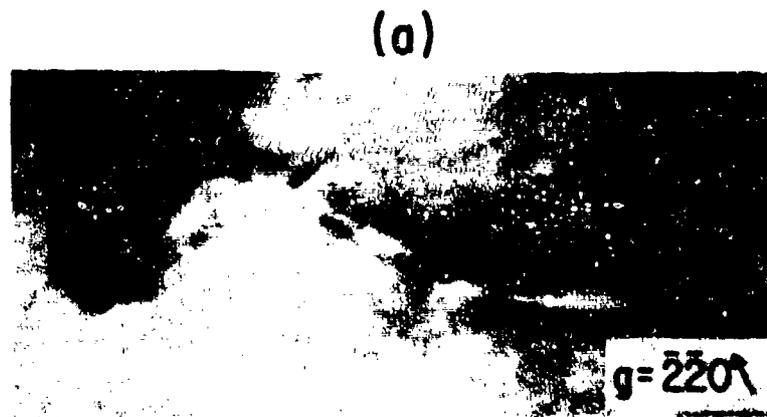
Figure 56   Partially Annihilated Stacking Fault. (a) Out of contrast.
(b) In contrast. (c) Dislocation assignments according to
Thompson notation.

99

1 μm

Figure 57 Unfaulting Shockley Partial Dislocations Nucleated from Dislocation
with Burgers Vector in Plane of Fault. Arrow 1 points to nucleating
dislocation (out of contrast) and arrow 2 to precipitates on other
out of contrast dislocations. Note residual fringe on unfaulted
plane (arrow 3).

plane into two Shockley partials [also out of contrast; see Figure 57(b)]. The configuration of these partials is such that the intrinsic fault between them annihilates the extrinsic oxidation stacking fault. Again note that the Shockley partials are curved into the stacking fault.

A most remarkable feature of this figure is the residual fringe visible where the fault has been annihilated. We see this residual fringe only when the stacking fault is annihilated by Shockley partials nucleated from a dislocation whose Burgers vector lies in the stacking fault plane. This contrast is indicative of the presence of an impurity adsorbed onto the stacking fault and left behind after the stacking fault has been annihilated. That this is the correct interpretation may be seen in Figure 58, where a partially annihilated stacking fault is imaged with $\vec{g} = \langle \bar{1}31 \rangle$. Under these conditions for a perfect stacking fault, $\vec{g}.\vec{R} = 1$, and the stacking fault is out of contrast. It will be seen that a weak fringe is still present on the stacking fault, and it is continuous across the freshly annihilated region. It should also be noted that the presence of the impurity plane clearly shows that the reaction is unfaulting the stacking fault.

The sense of the displacement across the plane of impurity atoms may be readily determined by comparing the sense of the black-white fringes with respect to the fringes on the stacking fault. Figures 57 and 58 show that the fringe in the unfaulted region is a weak continuation of the stacking fault fringe. Since the stacking fault is interstitial, the displacement causing the residual fringe is dilatational.

An estimate of the magnitude of the displacement was obtained by imaging several partially annihilated stacking faults formed at 950°C with the appropriate in-contrast 220 reflection, and under conditions of $s \approx 0$. Comparing the amplitude of the residual fringe with the amplitude of the stacking fault fringe, and using the calculations of Humphreys, et al.,[18] it

$$\vec{g} = 220$$ (a)

$$g = 13\bar{1}$$ (b)

0.5 μm
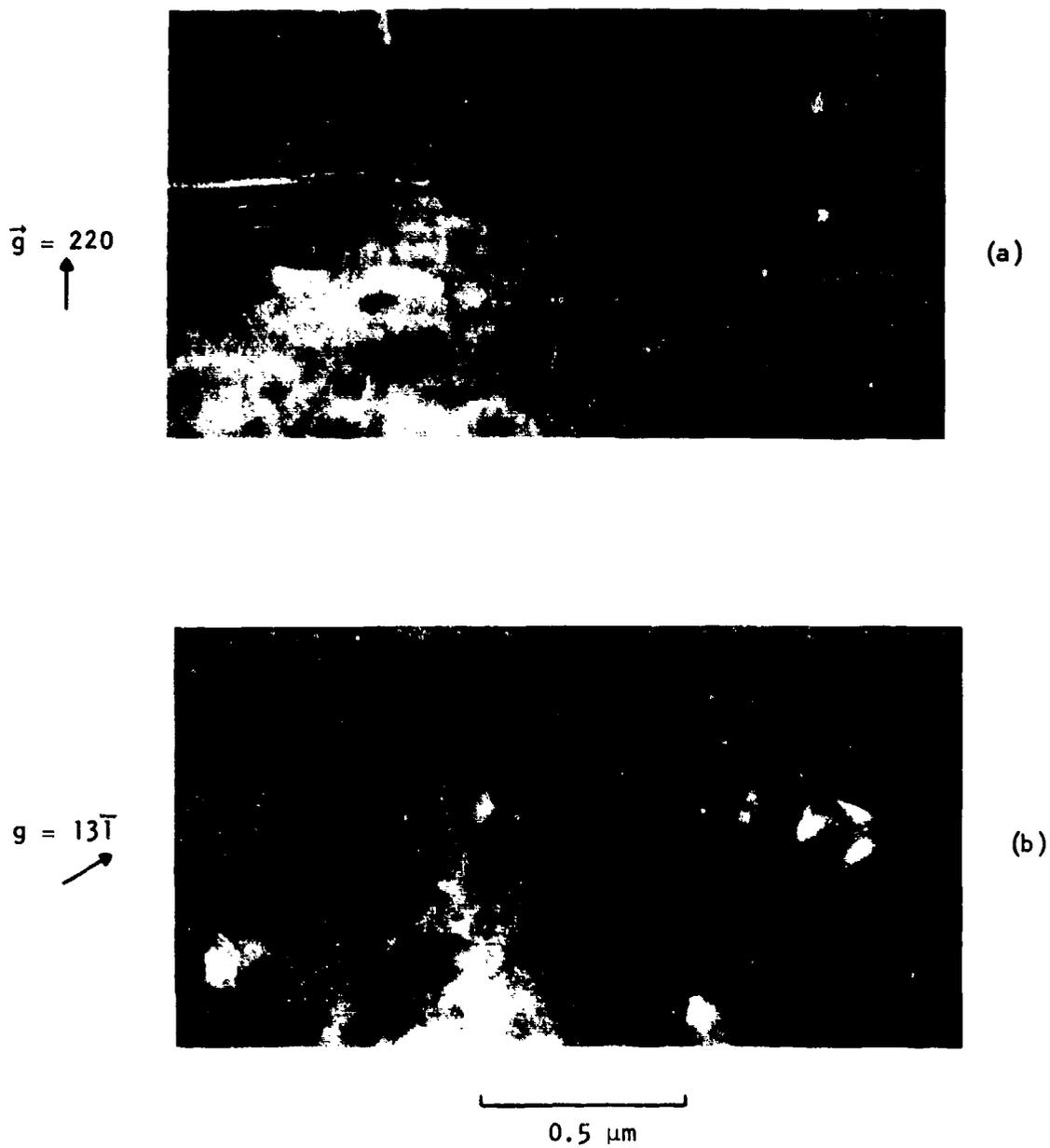
Figure 58 Weak Fringe on Unfaulted Region. (a) Stacking fault in contrast, (b) stacking fault out of contrast $(\vec{g} \cdot \vec{R} = 1)$. Note continuous weak fringe in (b) (above arrows) extending across both faulted and unfaulted regions.

was possible to estimate that $\vec{g} \cdot \vec{R}$ was from 0.03 to 0.10. No appreciable difference was detected in the magnitude of $\vec{g} \cdot \vec{R}$ of the residual contrast of partially annihilated stacking faults formed in the range of 900°C to 1100°C. Using the x-ray and STEM attachments of the JEOL-100CX microscope, we have been unable to detect any impurity on the stacking faults.

Attempts were made to destroy the impurity plane by heat treatment and subsequent TEM observation. Even after four hours at 700°C, no detectable change was observed in the intensity of the residual fringe (Figure 59).

While Figure 57 shows the nucleation of the annihilating Shockley partials from a dislocation whose Burgers vector lies on the plane of the stacking fault, Figure 60 shows the nucleation of a Shockley partial from a dislocation whose Burgers vector is not coplanar with the stacking fault. Figure 56 is evidently an example of the annihilation of an isolated stacking fault where the Shockley partial was nucleated within the stacking fault and not by an intersecting dislocation. Previous work has shown the existence of edge dislocations with the shape and size of stacking faults found nearby.[14]

In some cases we have found entire arrays of stacking faults in the process of unfaulting. An example of this is shown in Figure 61. From the four micrographs in this figure, the dislocation assignments of Figure 62 may be made. An interesting feature of these figures is a Shockley partial, indicated by the arrow in Figure 62, which is not curved into the stacking fault. This is the only case we have observed where the Shockley partial was not so curved.

Weak beam studies have been made on some of the unfaulting dislocation reactions (Figure 63). These confirm that the reaction does proceed as written in reaction (1), i.e., a Shockley partial and a Frank partial combine directly to form an undissociated perfect dislocation. It is expected that

0.5 μm

(a)

(b)
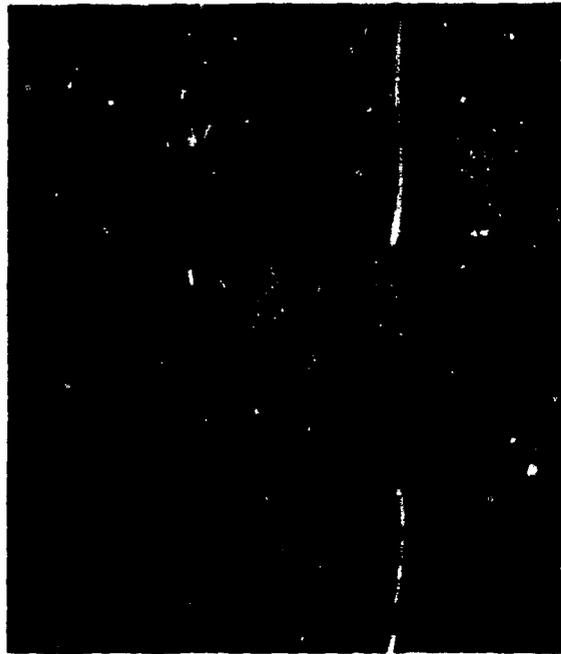
Figure 59   Residual Fringe Contrast.   (a) Before 700°C four-hour anneal.   (b) After 700°C four-hour anneal.   There is no detectable change other than the disappearance of surface dirt particles.

1 μm

Figure 60　Electron Micrograph Showing Shockley Partial (Arrow) Nucleated from the Reaction $1/2 \langle 110 \rangle + 1/3 \langle \bar{1}\bar{1}\bar{1} \rangle \rightarrow 1/6 \langle 11\bar{2} \rangle$.
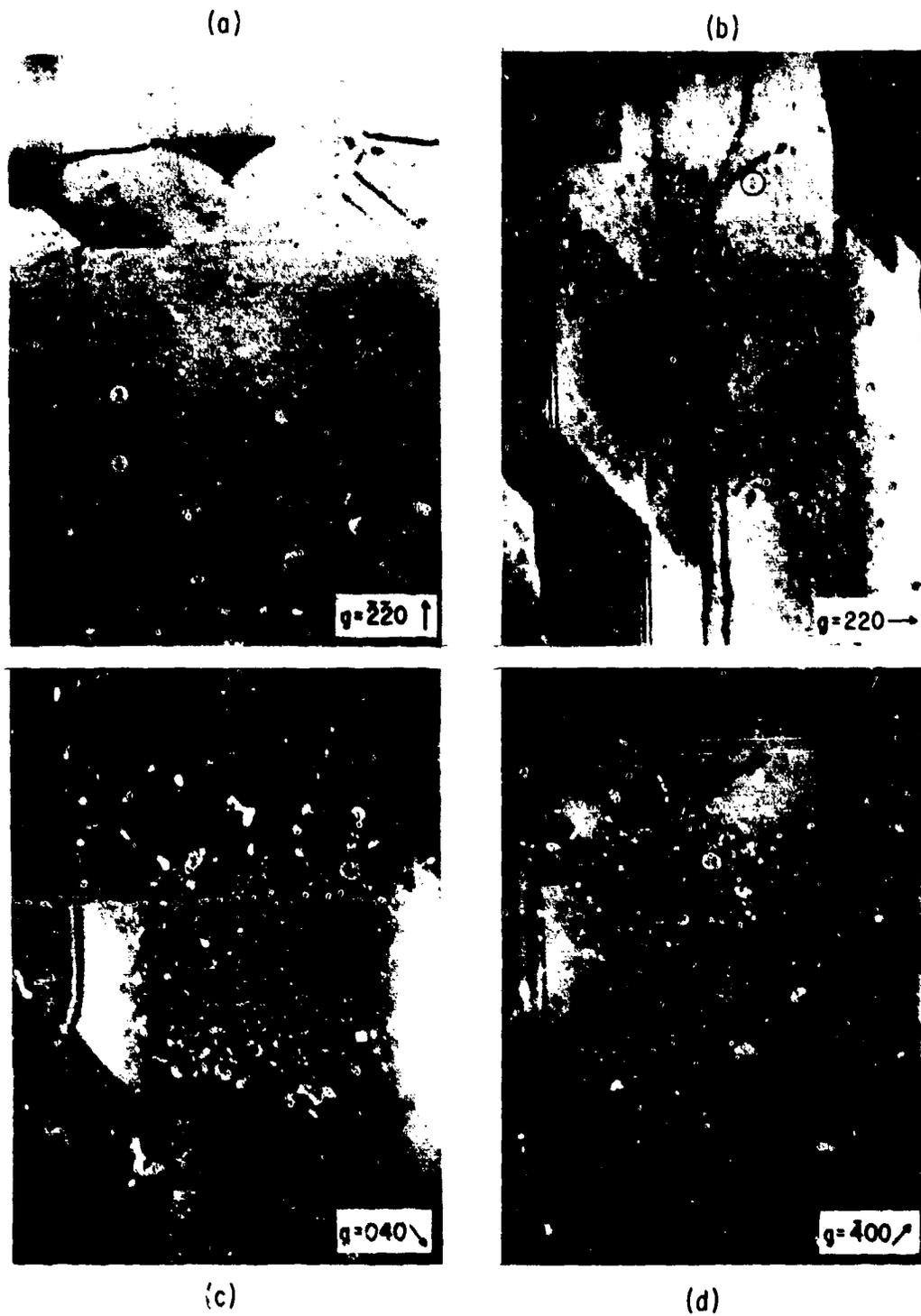
Figure 61 Micrographs of Partially Annihilated Stacking Fault Array. Note
residual fringe contrast, most visible in (a) and (b).
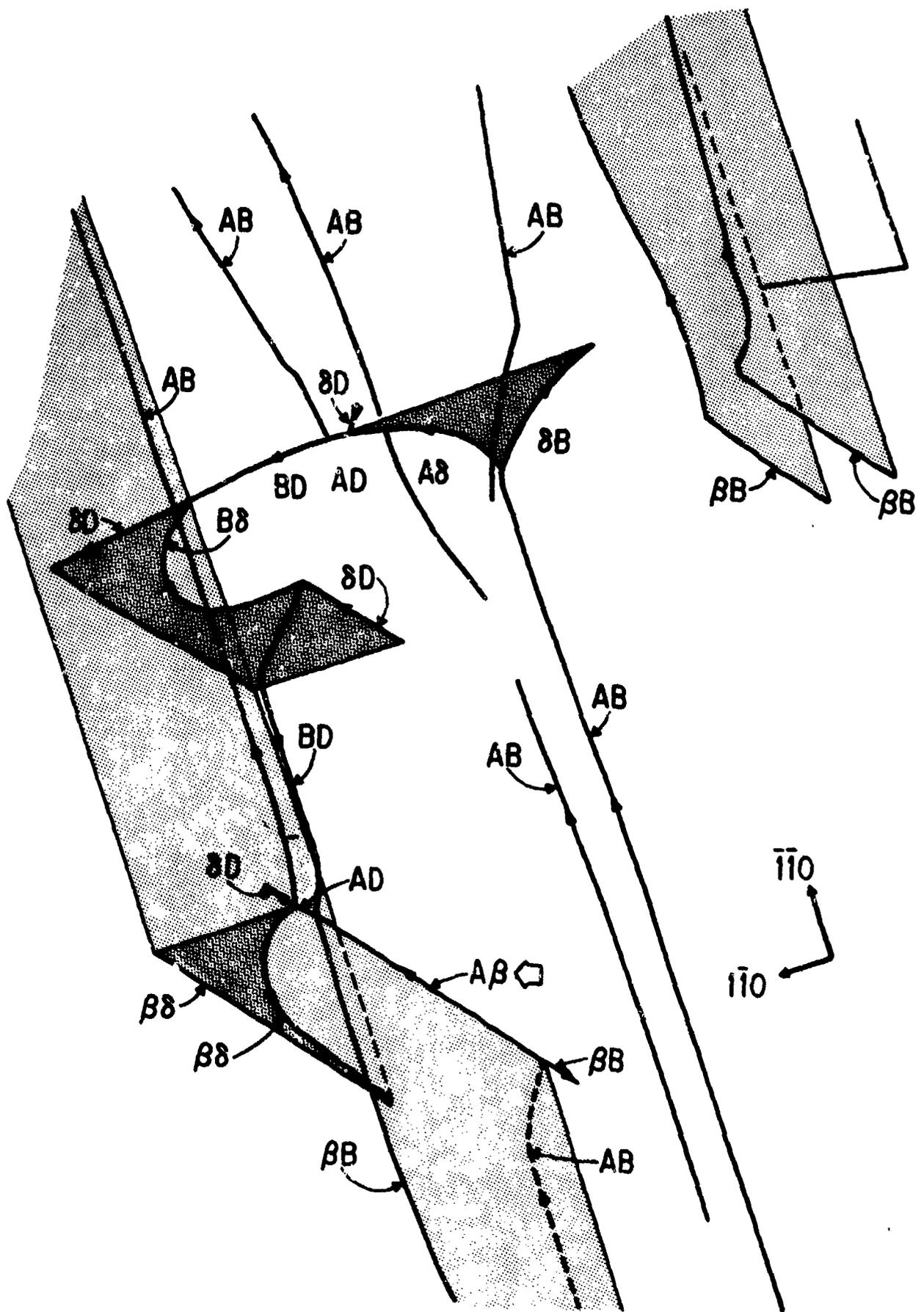
Figure 62   Dislocation Assignment of Figure 61 According to Thompson Notation

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50 nm

Figure 63 Weak Beam Micrograph of Unfaulting Reaction. The Shockley partial
bounds the stacking fault on the left, the Frank partial on the
right. The resultant perfect dislocation is undissociated except
at arrows. Note the dissociated edge dislocation in upper left of
the micrograph.

the perfect dislocation resulting from unfaulting will not be dissociated into two Shockley partials, since the perfect dislocation is, in general, not on a slip plane. However, portions of these dislocations and, in particular, the portions that intersect the crystal surface, are frequently found to be dissociated onto a (111) plane whose trace on the crystal surface is perpendicular to the original stacking fault (Figure 64). Through weak beam studies on many such dislocations, it can be stated that if a portion of one of these perfect dislocations is located on a slip plane, it will almost invariably be dissociated.

An interesting feature of these dislocations is that they are glissile and can be made to move in the electron beam. Figure 65 is a pair of weak beam micrographs showing the motion of a dissociated edge dislocation caused by focussing the electron beam to a spot ~100 nm. Direct observation confirmed that the dislocation remained dissociated during movement.

Occasionally, precipitation on dislocations was observed. An example of this is shown on the out-of-contrast dislocation in Figure 57. Only a very small number of dislocations showed evidence of precipitation (considerably less than 1%). Invariably, these were pure edge dislocations, and most were either obviously the result of recent unfaulting by virtue of the unfaulting reaction in process, or could be deduced to be recently unfaulted by virtue of their being the nucleus for unfaulting of other stacking faults (see Section V.D).

X-ray analysis of the precipitates in the STEM mode showed they contained copper (Figure 66). Weak beam studies revealed that the precipitates are apparently formed during the unfaulting of the stacking fault (Figure 67). Here, a series of very small precipitate particles can be seen on the perfect, undissociated dislocation formed by the unfaulting. It will also be noted that a very small (~10 Å) precipitate is being formed at the node where the
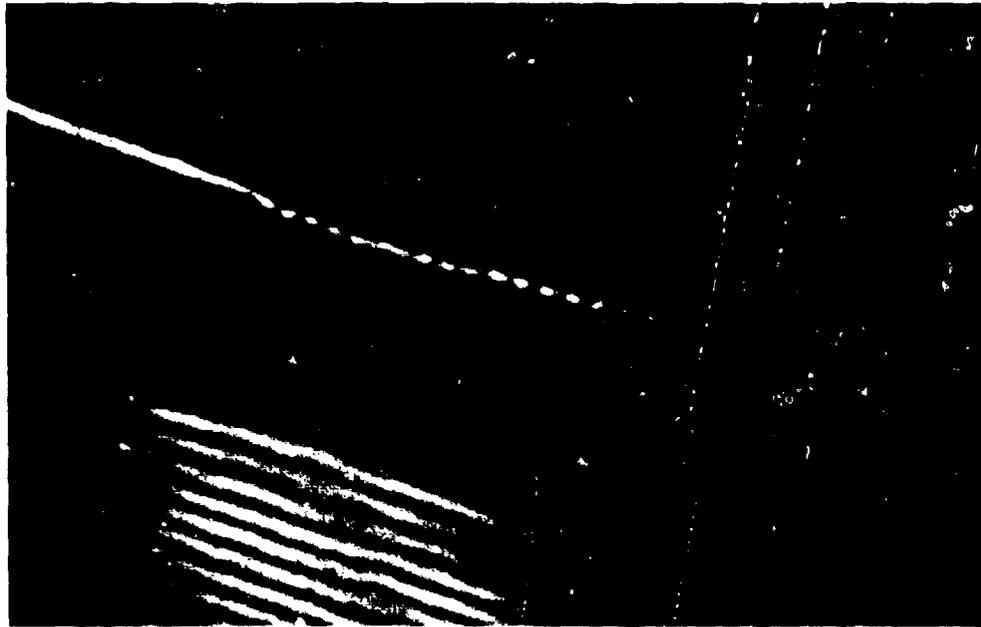
50 nm

Figure 64 Weak Beam Micrograph of Edge Dislocation. The end intersecting
the surface is dissociated on an inclined (111) plane. Fringe
contrast in lower left hand corner is from a stacking fault.

(a)

(b)

50 nm

Figure 65   Weak Beam Micrographs Showing Motion of Dissociated Dislocation
Under Beam Heating.   (a) Before heating, (b) after heating.   Direct
observation showed the motion occurred while the dislocation was
dissociated.

111
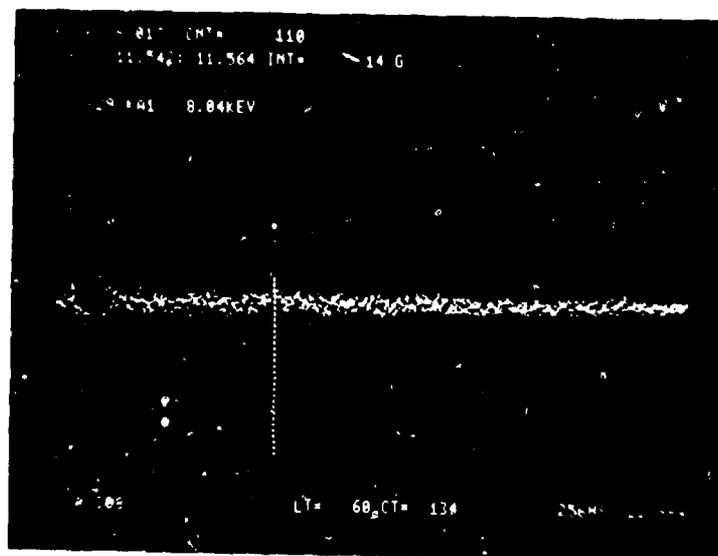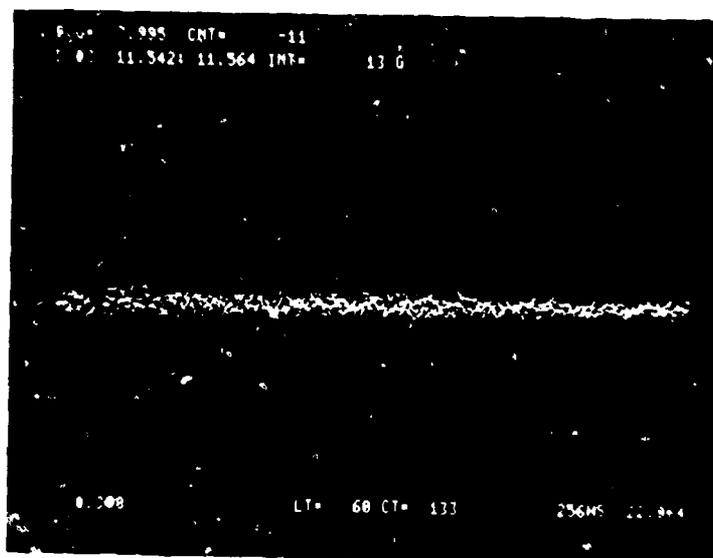
Figure 66   X-Ray Spectra.   (a) From precipitate particle, (b) from region next to particle.   Both spectra are the difference between the measured spectra and a spectra taken nearby.   Copper is detectable only in (a).

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Figure 67 Precipitation on Unfaulting Stacking
Faults. (a) and (b) Weak beam micro-
graphs. Note small precipitates on
dislocation that is imaged to either
side on the two micrographs. (c) Larger
precipitates showing Moiré fringe.

(a)   g = 220

(b)   g = 2̄2̄0

(c)   g = 2̄2̄0

50 nm

113
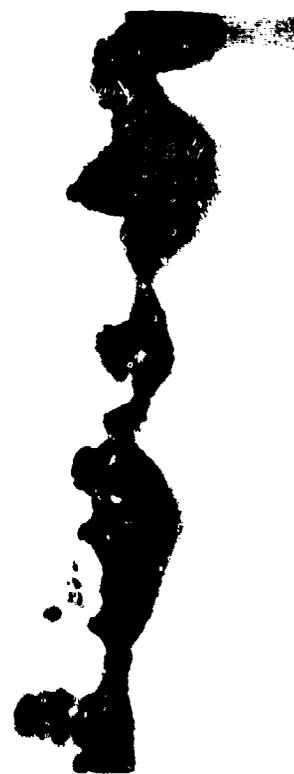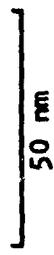
Shockley and Frank partials meet to form the perfect dislocation. Evidently, the Shockley partial moves in a series of jumps, and at each stop, the nucleation of a precipitate particle occurs at the dislocation node. Note that no precipitation occurs on either the Shockley or Frank partials. On larger precipitate particles, a fringe was frequently seen [Figure 67(c)]. This fringe spacing was found to be 45 Å. No diffraction patterns were observed from the precipitates.

On only a few occasions we have also seen precipitation on stacking faults (Figure 68). This has always been near the junction of the Frank partial and the oxide/silicon interface. Copper has previously been reported to precipitate in this fashion.[19] Precipitation in this manner is sufficiently rare (we estimate less than 1 in 10,000 stacking faults has precipitates) that we have been unable to verify the presence of copper by x-ray analysis. In contrast to Ravi and Varker's report,[14] we see no increase in the extent of precipitation after reoxidation, whether or not the first oxide is stripped.

In some regions of the samples, we find areas in which recent bulk nucleation of stacking faults has occurred (Figure 69). Occasionally, we also see peanut-shaped stacking faults such as in Figure 70. These stacking faults must be formed by the nearly simultaneous nucleation of two stacking faults on the same plane and grow together to form the observed shape. The simplest mechanism by which this simultaneous nucleation can occur is that the unfaulting of a previous-generation stacking fault leaves behind nuclei on which next-generation stacking faults can occur.

In contrast to stacking faults nucleated deep in the bulk, which invariably have a precipitate particle at the center of the fault,[5,6] the stacking faults we see here do not. Weak beam studies of these defects (Figure 71) with the stacking fault fringe ~60 Å in periodicity confirm the absence of particles $\geq$ 30 Å, since these would lead to a visible disruption of
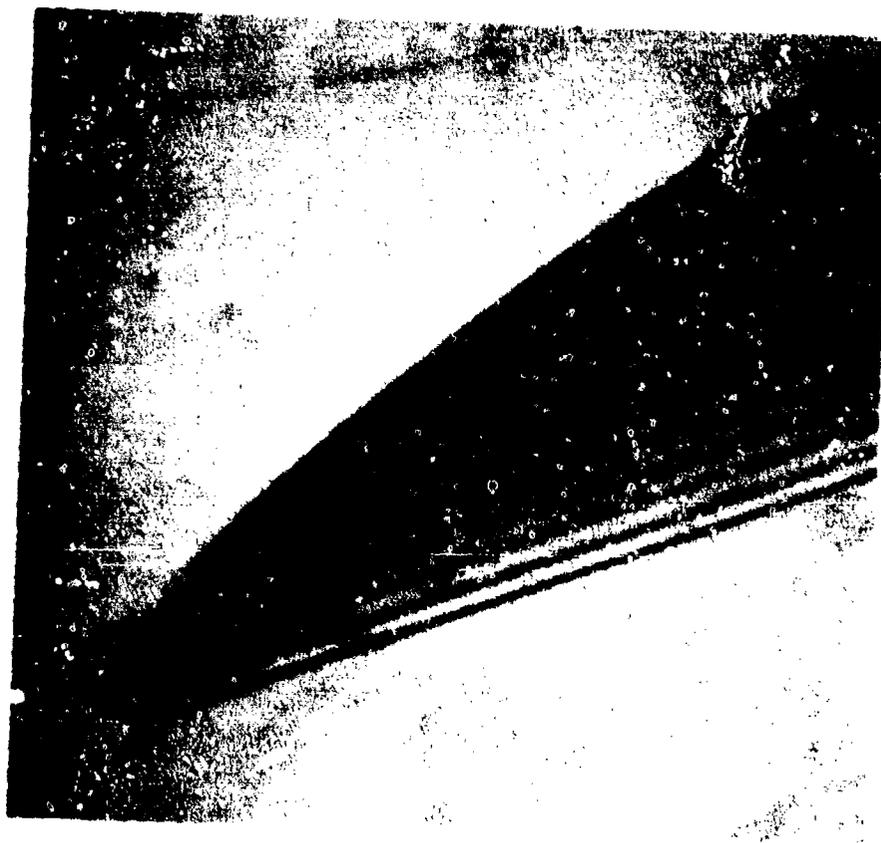
1 μm

Figure 68   Stacking Fault with Precipitate Colony at Edge

Figure 69 Subsurface Nucleation of Stacking Faults. Arrow indicates stacking fault in process of unfaulting.

0.5 µm

0.5 μm

Figure 70   Peanut-Shaped Stacking Fault

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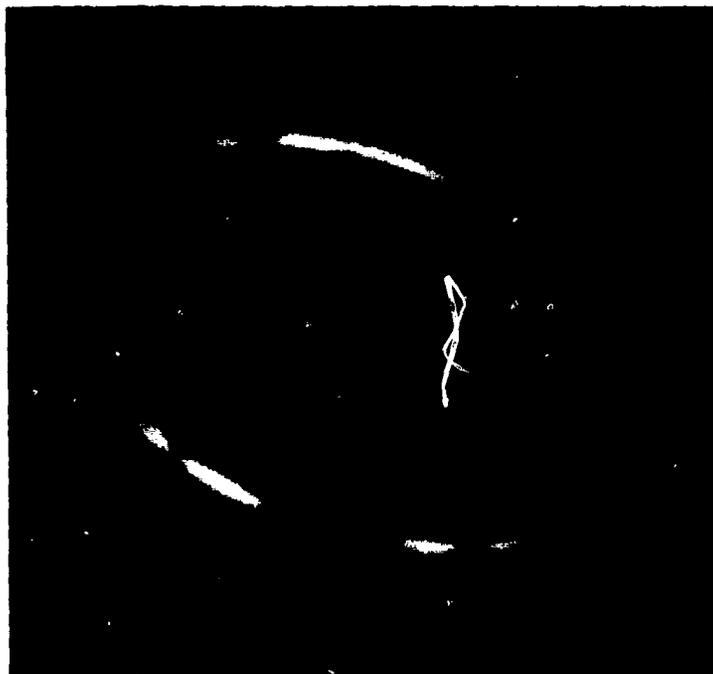
50 nm

Figure 71 Weak Beam Micrograph of Stacking Fault. Note continuity of fringe across fault.

fringe due to the change in the effective extinction distance of the electron beam in the precipitate particle.

D. Discussion

In all the unfaulting reactions we have observed, the Shockley partial has been curved into the stacking fault, indicating that the reaction is proceeding toward the unfaulting of the stacking fault. The unfaulting reaction proceeds to completion even in the presence of a copper precipitate particle, i.e., the dislocation observed near the precipitates is a perfect, undissociated dislocation rather than a pair of Shockley-Frank partials. This shows that the strain field of a copper precipitate partial is insufficient to prevent the formation of the perfect dislocation from the combination of the Shockley and Frank partials, and to cause the redissociation of the perfect dislocation, once formed, into the Shockley and Frank partials. It would therefore appear unlikely that if a perfect dislocation loop were formed in silicon, a faulting reaction could convert the loop into a stacking fault, even in the presence of a precipitate particle. Consequently, we would expect that a stacking fault would be nucleated directly as a stacking fault, and not through the faulting reaction of a perfect dislocation, as has been proposed.[5,6]

The unfaulting Shockley partial dislocation may be nucleated by another dislocation, or directly on the stacking fault. A residual plane of impurity atoms on the unfaulted region is observed only when the annihilating partials are nucleated by a dislocation whose Burgers vector is in the plane of the stacking fault. This indicates that this unfaulting occurs late in the cooling of the wafer, since the impurity plane does not have a chance to diffuse away. It is also consistent with the expectation that the nucleation of the Shockley partials is an athermal process. The dislocation responsible for this nucleation is a result of a previous unfaulting process, with the resulting dislocation lying on the (111) plane of the stacking fault. This

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dislocation immediately dissociates into the two Shockley partials in an intrinsic configuration, annihilating the extrinsic stacking fault. Note that the Burgers vectors of the perfect dislocations that are formed on completion of the unfaulting do not lie in the plane of the wafer surface for this process.

That a residual impurity plane is not observed when the Burgers vector of the resulting perfect dislocation lies in the plane ͜ the wafer surface indicates that this unfaulting process occurs only at higher temperatures where the impurity atoms do have time to diffuse away. This would be the case if the nucleation of the annihilating partial were to be a thermal mechanism. Figure 60 shows that when this partial is nucleated from a dislocation, a climb mechanism involving both the perfect dislocation and the Frank partial is required before a sufficient length of Shockley partial is generated to propagate and annihilate the stacking fault. Similarly, the nucleation of the stacking fault directly on the stacking fault plane is expected to be a thermally activated mechanism.

The observation of precipitation on some of the dislocations and the detection of copper in the precipitates provide much information on the effect of copper in small amounts. It will be appreciated that since these precipitates were confined to only a few dislocations, most of which could be directly determined to be the result of recently unfaulted stacking faults, the level of copper in the material is extremely small. Since no additional precipitation was noted after the 700°C anneal, it would appear that an upper limit of 5×10^{15} atoms/cm^3 can be placed on the copper concentration. (Note, however, that further precipitation may be kinetically limited at this temperature.) It appears that the contamination was introduced in the furnace in which the oxidations were carried out.

The mechanism for precipitation was observed. The precipitates were found to be nucleated at the node between the three dislocations during the unfaulting process. The obvious source of impurities for the precipitation process is the stacking fault. Then, as the unfaulting progresses, the impurities are swept up by a pipe diffusion mechanism on the Shockley partial to the precipitate site. We do not see precipitation on most defects of this same type, however. (Compare, for example, Figures 63 and 67.) If the defects with no precipitates were formed at higher temperatures than those with precipitates, then there are three possible explanations for the lack of precipitates:

(1) There are negligible impurities on the stacking fault at the higher temperatures.

(2) The unfaulting reaction at higher temperatures is sufficiently fast to disfavor nucleation, and hence the impurities diffuse away.

(3) The precipitates form due to the local supersaturation, but have sufficient time to redissolve.

There is direct evidence to support the second mechanism. In Figure 67 the spacing between precipitates decreases from left to right. Since the Shockley partial is also moving in this same direction, the temperature of the sample must have been higher when the precipitates at the left were formed than when those on the right were formed. The observed spacing is then consistent with a decreasing velocity of the Shockley partial with decreasing temperature, but with a less slowly decreasing nucleation rate.

Assuming the impurities in the precipitate particles are derived solely from the stacking fault, it is possible, from Figure 67, to estimate the concentration on the stacking fault. Since the images of the particles do not shift when the $\vec{g}$ vector is reversed in sign, while the position of the dislocation image does, the images of the particles can be determined to arise from the excitation of a diffracted beam from within the particles. The image

size is then the true particle size. Assuming an atomic volume of 12 $\overset{\circ}{A}^3$, and assuming all the atoms in a particle come from the stacking fault, then it is estimated that the concentration of impurities on the stacking fault must have been of the order of 1.7×10^{14} cm^{-2}.

It should be noted that the mode of precipitation we observed must be the easiest mode, since no precipitation is observed on either the Shockley partial or the Frank partial.

We next consider the question of what impurity causes the residual fringe contrast and hence is found on the stacking fault. A lower estimate for its concentration may be made by assuming that its volumetric expansion is equal to the volume occupied by 1 atom of silicon, i.e., 2×10^{-23}. Since displacement is observed only in a direction normal to the (111) plane on which the impurities are located, it is most probable that the impurity is located on the bonds normal to this plane. Using the values of $\vec{g} \cdot \vec{R}$ in the last section, it is then possible to estimate that the concentration is from 2×10^{14} to 4×10^{13} cm^{-2}, which is equivalent to a concentration of from 6×10^{20} to 1.2×10^{21} atoms/cm^3 on the single stacking fault plane. Clearly, this is a large concentration, and the only impurities that could be available in such concentration are oxygen and copper. The above concentration estimate is probably considerably smaller than the concentration that is present, due to a conservative value for the volumetric expansion. Oxygen, for example, has a reported value of 4.5×10^{-24}.[20] Using this value, the concentration on the stacking fault would be of the order of 9×10^{13} to 1.8×10^{14} cm^{-2}. A corresponding volumetric expansion coefficient is not available for copper. This latter value is surprisingly close to that estimated for the concentration required to give rise to the precipitates.

We are now in a position to propose a consistent model that explains the disposition of the impurities as unfaulting occurs at various temperatures.

At the highest temperatures, the reaction proceeds so fast that the nucleating process does not have time to take place. The residual impurities diffuse away, and no precipitation occurs. At intermediate temperatures the velocity of the partial is slow enough to allow nucleation at the dislocation reaction node. Diffusion of the impurities to the precipitate then occurs via pipe diffusion (or possibly across the stacking fault plane). The reason the precipitates are formed on the edge dislocation (or rather, as careful examination of Figure 57 shows, ahead of the dislocation) is that this dislocation can accommodate the interstitials produced by climb. As the temperature is reduced further, either the diffusion rate of the impurities or the climb rate of the dislocations is sufficiently small that the motion of the Shockley partial proceeds, leaving behind the impurity plane, and again, no precipitation occurs. This low temperture stage is never observed when the Shockley partial is nucleated by a thermally activated process -- the unfaulting is complete (or nearly complete) by the onset of this stage. The small segments of unfaulted stacking fault that we observe in this case evidently result from a pinning of the Shockley partial before the last temperature stage is reached. All of this occurs at T > 700°C.

The observed stability of the residual impurity plane at 700°C seems inconsistent with the impurity being only copper, however. It would appear that four hours at this temperature, during which the diffusion length of copper is 1 cm, would be sufficient to cause the complete dissolution of the plane, or at least the formation of precipitate platelets. Consequently, we believe that the impurity plane is mainly oxygen. This would also mean that the precipitate particles also contain oxygen. The observed Moire fringe contrast seen on the larger particles lends support to this supposition. An identical fringe contrast has been seen by Bialas and Hesse[21] for precipitates of SiO_2 on dislocations in silicon. It is indicative of an interplanar spacing of 1.92 ± 0.08 Å in the precipitate particle, in agreement with the spacing of 1.85 Å found in several phases of SiO_2. Under these circumstances,

the occurrence of copper in the precipitate may be incidental to the formation of the precipitate. The copper is "gettered" into or onto the precipitate particle.

Attempts were made to determine the stacking fault energy of the "dirty" stacking fault by measuring the radius of curvature of the Shockley partial dislocation. The values were found to range from ~ 300 Å to 1 µm for the radius of curvature. The largest values were found for Shockley partials that left behind an impurity plane. These dislocations were obviously arrested in motion by the cooldown of the sample and therefore are not in equilibrium. The smallest value was found on defects that can reasonably be expected to be in equilibrium, for example, the partial dislocations in Figures 60 and 67. The calculation of the stacking fault energy from this radius of curvature leads to a value greater than that reported for the extrinsic stacking fault,[10] however. This is an indication that there is an additional stress acting on these dislocations. A stress caused by the lesser thermal expansion coefficient of the surface silicon oxide with respect to that of the silicon would lead to a stress of the proper sign to cause increased bowing of these partial dislocations. It is therefore impossible to measure the stacking fault energy in our samples. It should be emphasized, however, that the energy of the stacking fault with an adsorbed impurity must be less than that of a clean fault. In fact, some recently reported anomalies on the dissociation of screw dislocations in silicon show that the extrinsic stacking fault energy in silicon can be lowered, probably by the adsorption of impurities onto the stacking fault.[11]

It should be noted that residual contrast has been previously reported on stacking faults when $\vec{g} \cdot \vec{R} = 1$ for a perfect stacking fault,[5,22] indicating that the extrinsic stacking fault resulting from oxidation or precipitation is dirty.

We are now in a position to understand the nucleation of new stacking faults that is observed. When a previous stacking fault is annihilated at high temperature, it leaves behind the adsorbed impurities, initially on one plane. Evidently, the oxygen and copper left behind can nucleate the new stacking fault in the presence of excess interstitials produced by the oxidation at the surface. The role of oxygen in this nucleation process is fairly clear; it suppresses the stacking fault energy of the resulting defect, making the collapse of the interstitials into a stacking fault feasible. The role of copper is less clear. Perhaps it serves as the "glue" to hold everything together until the stacking fault is formed.

SECTION VI
DISCUSSION

This section contains a review of the electrically active defects that have been observed and a discussion of their probable origins. A model for electrical activity from dislocations is proposed that is consistent with our observations. Finally, we present a discussion of gettering mechanisms based on our observations of the effects of gettering in devices, as well as on the results of Section V.

A. Origins of Electrically Active Defects in CCD Imagers

1. Dislocation from Unfaulted Subsurface Bulk Stacking Fault

This is the most prevalent type of dark current producing defect, and evidence for it was found in almost all the material investigated. The occurrence of these defects appears well correlated to both faulted and unfaulted stacking faults in the channel stops. From five to ten times as many defects were found in the channel stops as in the channel. In the imager, these defects gave rise to a locally random distribution of dark current spikes, most of very low level, with some having moderate level. The defect size ranged from 0.1 μm to $\sim$ 10 μm. Most were 1 μm or less in length.

We have found that the length of stacking faults nucleated at the beginning of the process is 9 μm in the channel stop, $\sim$ 1.3 μm in the center of the channel, and up to 7.5 μm at the edge of the channel. The variability in length that was observed in devices not intentionally damaged clearly indicates they are nucleated throughout the process. Thus, this defect appears to be the same as that previously reported to be the most pervasive in CCD imagers.[23,24] It should be noted that our investigations, which have been a more thorough characterization than the etching studies that have been used,

reveal that the defect in the channel is an unfaulted stacking fault, at least in our device.

The fact that the smaller defects are more numerous, particularly under the channel stop oxide, suggests that the largest number of these defects are nucleated late in the processing cycle. In particular, it would appear that most of them are nucleated before or during the growth of the oxide underneath the polysilicon gate.

Even though they are nucleated in the bulk, these stacking faults are clearly different from bulk stacking faults found deep in the slice and those associated with bulk swirl precipitation in that no central precipitate is found on the stacking fault.[5,6] Furthermore, all of them are nucleated close to the oxide/silicon interface. In this respect they are identical to the freshly nucleated stacking faults discussed in Section V.

A plausible scenario for the development of these defects requires the hypothesis of the nucleation mechanism. Two mechanisms seem reasonable:

(1) That copper acts as a nucleation agent for stacking faults. This possibility was discussed in Section V. The observed size distribution would then follow from an increased copper concentration during processing and/or the failure of intrinsic and backside gettering mechanisms in the process. In either event, the increase in the amount of copper available would result in an increased nucleation rate later in the process.

(2) That carbon acts as a nucleation agent for stacking faults. There is some indirect evidence implicating carbon as a source of defects such as stacking faults.[25,26] The observed size distribution would then result from the diffusion of carbon to the surface during processing, and the subsequent increased concentration available for nucleation.

In either event, it should be recognized that the nucleation must require several impurity atoms; otherwise, there would be many more stacking faults than are actually observed. The requirement for several atoms would lead to a nucleation rate proportional to some power of the concentration of impurities and, hence, would be strongly reduced with decreasing concentration. In addition, it seems likely that a supersaturation of oxygen and/or a supersaturation of silicon self-interstitials are also required for the nucleation to take place.

It should also be noted that a 700°C anneal is effective in nucleating stacking faults in Czochralski silicon.[27] All commercial Czochralski silicon (including that used in this study) receives an anneal in this temperature region to stabilize the resistivity while the crystal is still a boule. Since the nuclei, once formed, are stable at high temperatures, it appears likely that some of the large stacking faults are a result of this stabilization bake.

2. Process-Induced Dislocations

The types of process-induced dislocations include the familiar thermal stress dislocations, which are generated by thermal gradients during slice cooldown[28]; and dislocations generated at the center of the backside during processing, which are propagated to the frontside. Our results indicated that both float-zoned and backside-damaged Czochralski slices are more susceptible to the formation of these defects than are conventional Czochralski wafers.

Recently, Hu[29] has shown that dislocations are able to move under lower stresses in oxygen-free silicon than in silicon with oxygen. This would explain the behavior of the float-zoned material. Lacking oxygen, for a given stress source, the dislocations can propagate further to a region where the

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stress is lower than they can for an identical stress source in Czochralski silicon.

The behavior of backside-damaged silicon would suggest that the stresses introduced by thermal stresses or backside process damage are added to the stresses introduced by the backside damage process. While neither of these alone is sufficient to cause a problem, together they result in numerous dislocations at the frontside of the device.

3.   Device Stress Dislocations

These dislocations are shallow dislocations found in the channels and channel stops. In Section IV it was shown that these dislocations are formed during the thick oxide growth step, probably during cooldown. They are glide dislocations and move under the stress of the thick oxide, which exists due to the differences in the thermal expansion coefficients of silicon and silicon dioxide. The overlying polysilicon also exerts a stress field that has been found sufficient to remove shallow-lying channel/channel stop dislocations from the silicon, and in some instances to generate short segments of dislocation perpendicular to the channels and channel stops.

Two nucleation mechanisms have been observed for these dislocations:

(1) From a preexisting dislocation. These dislocations may be thermal stress dislocations or dislocations formed subsurface during the bulk swirl precipitation of oxygen.

(2) From a scratch. Since a scratch is usually converted into a series of stacking faults during the initial oxidation, the source of the dislocation is probably an unfaulted stacking fault.

Since these are glide dislocations, their movement is confined to (1$\bar{1}$1) planes. Consequently, they may be effectively controlled by placing the

channels and channel stops (and the polysilicon electrodes) in ⟨100⟩ directions. In this manner, (111) planes are no longer parallel to the stress field of the thick oxide or polysilicon, and dislocation propagation is not favored. In fact, we have never seen this type of defect in samples with a ⟨100⟩ flat.

4. Atomistic Defect

This defect produces regions of higher dark current that have been characterized as dark current banding. Most interesting is the fact that the appearance of dark current banding has invariably been associated with the nearly complete absence of dark current spikes. It has been found to be getterable at short range (< 50 μm).

5. Surface Defect

This defect was deduced to be located at the silicon – oxide interface, since no defect that was observed in the electron microscope correlated with the dark current defect in the imager. This defect is getterable by backside mechanical damage. It has been found at the periphery of bulk swirl precipitation, and only when dark current banding is not present.

6. Stacking Faults

Stacking faults in the channels have been observed in this work only when the stacking fault was nucleated from a scratch. Stacking faults nucleated by another mechanism (or mechanisms) have always been found to have unfaulted in the channel. Stacking faults in the channel, however, have been found to be a source of dark current.

B. Electrical Activity of Dislocations

A marked difference in the electrical activity of dislocations has been noted in this study. In particular, we find that very few dislocations that originate by a glide mechanism are dark current sources, while our data

suggest that almost all dislocations resulting from the unfaulting of a stacking fault are dark current sources. While we do not have a definite count, our observations on the electrical activity of glide dislocations is in agreement with published accounts that only 5% of these dislocations are electrically active.[23,30]

In the first place, it is clear that a dislocation must be in the depletion region of a device if it is to be a dark current source, since dislocations located just outside the depletion region, created by bulk swirl precipitation, are not dark current sources. The depletion region extends to a shallow region under the channel stop, and an electrically active dislocation has been found here. The surprising feature is that dislocation from unfaulted stacking faults, which are seldom more than 1 μm in length, are dark current sources, while glide dislocations that have at least 5 μm in the depletion region are not dark current sources.

It should be pointed out that no precipitates have been found on any defect in devices in this work. The behavior of copper precipitates in weak beam experiments on defects in nondevice samples enables us to conclusively state that in devices, no copper precipitates larger than 5 $\overset{\circ}{A}$ diameter are present. Thus, it appears that precipitation can be ruled out as the cause of observed electrical activity.

A possible explanation for this behavior results from the weak beam experiments conducted in the electron microscope on these dislocations. In particular, we find that most glide dislocations are dissociated into two Shockley partial dislocations, while all dislocations resulting from the unfaulting of a stacking fault are undissociated. Thus, a simple explanation is that undissociated dislocations are dark current sources, while dissociated dislocations are not.

Hirth and Lothe[31] show that two types of dislocations are possible in silicon. They name these the "shuffle" and "glide" sets of dislocations. Examination of ball and stick models of these dislocations (Figure 72) shows that the dangling bonds formed on the glide set of dislocations may be healed by the formation of five and seven rings (rather than the normal six rings found in the perfect crystal), while the dangling bonds on the shuffle set may be joined only by the formation of three rings. The formation of three rings would appear energetically unfavorable because of the large strain associated with their formation. Thus, if the dissociated dislocations we observe belong to the glide set, their core structure could have no dangling bonds, thus accounting for their electrical inactivity. If the undissociated dislocations belonged to the shuffle set, then the dangling bonds, or the adsorption of impurities to the dangling bonds, could account for their electrical activity. Conversion of the electrically inactive glide dislocation to an electrically active dislocation could then occur either through constriction of the two partials into an undissociated dislocation, or possibly, as has been recently discussed, through the conversion of one of the partials from the glide set to one of the shuffle set, by the application of suitably high stresses at low temperatures.[32]

Based on the observed dark current and the length of dislocation, we estimate that the undissociated dislocation resulting from the unfaulting of a stacking fault results in a leakage of 1 to 5 nA/cm of dislocation line in the depletion region.

C. Effect of Gettering on Dark Current Defects

We have observed gettering by two different mechanisms: by backside mechanical damage, and by intrinsic gettering by the bulk swirl precipitation of oxygen. Their effectivensss on various defects is summarized in Table 5. Clearly, backside mechanical damage has been dissappointing as a gettering mechanism. Bulk swirl precipitation, on the other hand, appears much more
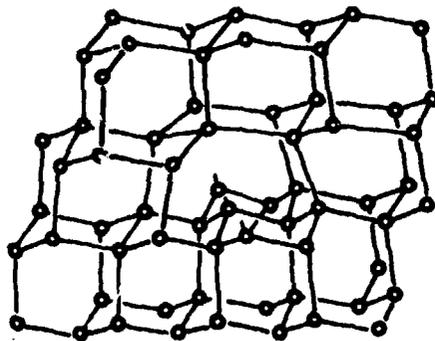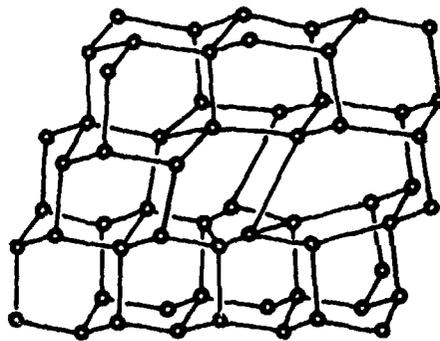
Figure 72 Models of 60° Dislocations. (a) Glide set, (b) shuffle set. The dangling bonds in (a) may be healed pairwise (heavy line) by the formation of five and seven rings. In (b) they may be healed only by the formation of three rings.

Table 5

Summary of Gettering Effects on CCD Imagers

Defect	Effects of Backside Damage	Effect of Bulk Swirl Precipitate	Remarks
Subsurface Bulk Stacking Faults	Slight	100% possible	-
Process-Induced Dislocations	Aggravates	?	Precipitation hardening has been observed
Device Stress Dislocations	No effect	No effect	⟨100⟩ flat confines to single pixel
Surface	Effective	Effective	
Atomistic	No effect	Effective if swirl is close to surface	
Stacking Faults/ Scratch	No effect	No effect	Preprocess anneal in nitrogen appears effective

effective as a gettering mechanism. In fact, the best imagers in the present study, with by far the fewest dark current defects, have been found over regions where the bulk swirl precipitation of oxygen has occurred. The converse is not true, however. We have seen imagers over bulk swirl precipitation that had a moderate number of dark current defects.

Certainly our work shows that backside mechanical damage does no harm, provided the process takes into account the greater susceptibility of this material to the generation of process-induced dislocations.

It is interesting that backside mechanical damage has not been effective. It should be noted that most reports of the effectiveness of backside damage follow it only through a single oxidation.[1,33] In these cases, it is found that backside damage strongly reduces the occurrence of stacking faults. It should be noted that we see very few large stacking faults in the devices. Most are very small, indicating nucleation late in the process. Thus, backside gettering may be initially effective, but loses its effectiveness as processing continues.

The damage introduced on the frontside and reported in Section V can be viewed as a gettering mechanism; as such, it provides us with an explanation of the failure of backside damage. In particular, we find that copper does not precipitate on dislocations. We find copper in (or on) precipitates of oxygen on dislocations. These precipitates are formed in a very narrow temperature range on cooling the wafer. From these results, we can develop a scenario for the gettering of copper in silicon.

(1) Copper is at best adsorbed to dislocations in silicon. From the previous section on the electrical activity of dislocations it would appear that copper can be adsorbed only on undissociated dislocations. It should be

emphasized that the generally observed electrical inactivity of slip dialocations is incompatible with these dislocations gettering copper.

(2) The preferred gettering site for copper is an oxygen precipitate. In Section V it was seen that these precipitates were formed in conjunction with the unfaulting of a stacking fault during cooldown, and from the local supersaturation produced by the oxygen adsorbed on the stacking fault.

(3) The main role of dislocations in backside gettering is to provide sites on which oxygen precipitation takes place. In order for this precipitation to occur, however, there must be a supersaturation of oxygen. This condition is met during the initial oxidation of silicon, but as the oxidation progresses, the supersaturation of oxygen decreases due to out-diffusion of oxygen to the backside. Thus, after the first oxidation, the precipitation of oxygen ceases, since there is no more oxygen to precipitate. Thus, the gettering action ceases to be effective.

(4) The ability of dislocations to adsorb copper will also undergo a reduction with time as the array tends toward the lowest energy form of dissociated dislocations.

(5) In contrast to the backside mechanism, the bulk precipitation oxygen has two advantages: it involves all the oxygen in the slice, and hence is capable of gettering more copper; and it is continuous throughout the process, since the oxygen deep in the bulk cannot out-diffuse as can that near the backside.

SECTION VII
RECOMMENDATIONS

From the foregoing data and discussion, it should be clear that the starting material and the fundamental process are inextricably connected. Deficiencies in the material that are presumably insufficient to cause dark current spikes by themselves develop into dark current producing defects during processing. In addition, since stacking faults may be nucleated by trace amounts of copper, and since trace amounts may be added to the material during processing, the material may also be required to make up for inherent deficiencies in processing by providing electrically inactive regions to place this copper.

The prevention of defects in the completed device may then logically proceed by the specification of material able to cope with an existing process, or by a radical change in the processing, either by modifications to an existing process, or by the development of a new process that is inherently defect-free.

A. Recommendations for the Selection of CCD Material

(1) Material that produces bulk swirl precipitation of oxygen is the best material for the fabrication of defect-free CCD imagers. In this study, the best imagers have been produced on this material.

(2) Backside gettering has a slightly beneficial role. In this study backside gettering either has led to a reduction in the number of dark current spikes, or has had no effect. Degradation has been noted only when problems were encountered in processing as discussed in Section III.C.3.

(3) The orientation of a device on the wafer such that channels and channel stops are parallel to ⟨100⟩ directions suppresses the formation of dislocations caused by device stresses.

B.   Recommendations for Material Research

(1)   Determine the requirements of material to produce bulk swirl precipitation of oxygen. Clearly, one requirement is that the wafer contain a large amount of oxygen. However, our experience has shown that this is not a sufficient requirement; wafers with large amounts of oxygen do not always produce bulk swirl precipitation when subjected to the process. It appears that the precipitation we observe is heterogeneously nucleated.

(2)   Determine the effect of eliminating the stabilization bake currently used to stabilize the resistivity of silicon boules. There are indications that this procedure can lead to the nucleation of stacking faults in the device region.

(3) Determine the role of carbon in nucleating defects. There are indications that carbon may be associated with the nucleation of defects such as stacking faults in the device. If so, a low carbon specification would be in order.

(4) Determine specifications and a quality control screen for low-defect material. A quality control screen would consist of a sequence of oxidation/anneals to produce defects that correlate with those developed in the process. Because many of the defects are nucleated late in the process, it is unlikely that a single oxidation or anneal will be capable of developing sufficient evidence on material quality.

(5) Determine the most effective backside gettering technique. In this work we have explored only backside mechanical damage as a gettering technique. Our results indicate that it loses its effectiveness early in the process. It is not clear whether this is the case for all backside gettering techniques. If intrinsic gettering by the precipitation of oxygen can be made to work, however, the case for backside gettering could be reduced.

C.   Recommendation for Modifications to Existing Process

A two-step gettering procedure prior to the growth of the channel gate oxides may alleviate the problem of stacking faults (both faulted and unfaulted) in the channel region.

(1) An anneal under a neutral or reducing ambient with all channel oxide removed. This should annihilate existing stacking faults and dislocations from unfaulted stacking faults by allowing them to climb to the surface. The climb proceeds most rapidly in the absence of a thermal oxide.

(2) The application of an additional backside gettering process after the anneal. The purpose of this gettering would be to provide a renewed backside gettering to prevent the subsequent growth of stacking faults during the formation of the gate oxide.

D.   Recommendations for a Future Defect-Free Process

Our results clearly show that the degrading defects are formed during thermal oxidation steps. Furthermore, the thermal oxide, when present, acts as a mirror to silicon self-interstitials during subsequent nonoxidizing anneals. This prevents their being annihilated at the surface. As discussed in Section IV, there are indications that chemically deposited oxide does not possess this peculiar property of a thermal oxide.

It would therefore seem logical to minimize the use of thermal oxidation steps to reduce the formation of defects. It is suggested that chemically deposited oxides be investigated for use as diffusion or implantation masks. The use of high pressure thermal oxidation at lower temperatures may serve to reduce the growth of defects when the electrical properties of a thermal oxide are required.

It would appear that the optimum situation would be to have both material that is capable of producing imagers with low dark current defect density and a process that minimizes the probability of producing these defects.

APPENDIX A
CRYSTALLOGRAPHIC DEFECTS IN SILICON

A brief summary of the crystallographic defects that are discussed in the body of the text (dislocations and stacking faults) is given in this appendix to allow the reader who is unfamiliar with the terminology used in the body of this report to follow the discussion. Key terminology is therefore underlined. For more detailed discussion, the reader is referred to the books by Hirth and Lothe,[34] and by Nabarro.[35]

A.   Dislocation

The formation of a dislocation in a solid is illustrated in Figure A-1. Beginning with a solid continuum block (a), a cut is made partially through the block along a plane (b). Then the portion of the block above the cut is shifted to the left and the portion below to the right (c). The two portions of the block above and below the cut are then rejoined to give rise to the dislocation in the continuum, which is located where the cut plane stopped (d). The shift of the portion of the block above the cut with respect to the portion of the block below the cut is called the Burgers vector of the dislocation and is labeled $\vec{b}$ in Figure A-1(d). In this figure the shift has been made perpendicular to the line of the dislocation (which runs perpendicular to the plane of the figure), and the resulting dislocation is called an edge dislocation. Note that the Burgers vector may make any angle to the dislocation line simply by shifting the top portion of the block in an appropriate direction with respect to the bottom before the cut plane is rejoined. In particular, if the Burgers vector is parallel to the dislocation line, it is called a screw dislocation.

The situation in a crystal is schematically illustrated in Figures A-1(e) and A-1(f). Because of the periodicity of the crystal lattice, when the top and bottom halves of the crystal are rejoined, continuity of the
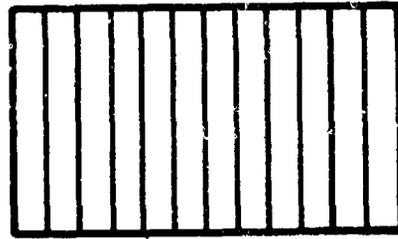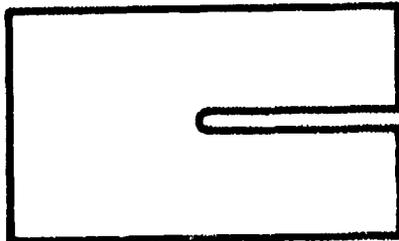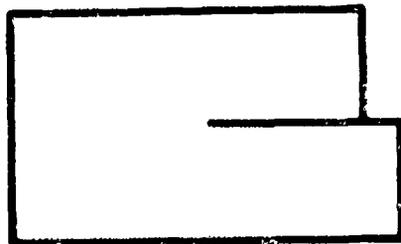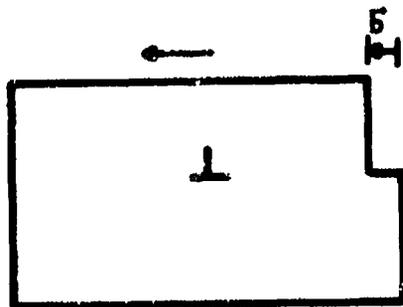
Figure A-1 Dislocation in a Solid

atomic bonds can be achieved only for a few specific values of the Burgers vector.

There are two ways in which a dislocation may move in a crystal. If the plane of the cut is an allowed slip plane [in silicon, the allowed slip planes are (111) planes], then under the application of a shear stress as indicated by the arrows at the top and bottom of Figure A-1(d) the dislocation will move to the left. This process is called slip or glide, and the dislocation is called glissile. Note that the slip plane is the plane containing both the dislocation line and the Burgers vector. The dislocation may also move perpendicular to the slip plane by adsorbing or emitting atoms from its core, where the extra half plane of atoms ends [Figure A-1(f)]. This process is known as climb. Dislocations for which the dislocation line and Burgers vector do not fall on an allowable slip plane can move only by climb and are called sessile.

Two general classes of dislocations may be found in a face centered cubic crystal such as silicon: perfect or partial. A perfect dislocation is one in which the crystal surrounding the dislocation is perfect, i.e., retains the cubic symmetry, except for distortions created by the discontinuity at the dislocation core. A partial dislocation is one in which the cubic symmetry is destroyed by the presence of a stacking fault (see below) on one side. In silicon the Burgers vectors of perfect dislocations are of the type a/2⟨110⟩, where a is the lattice parameter.

B. Stacking Fault

In a face centered cubic material, (111) planes of atoms are stacked in a three-layer sequence such as illustrated in Figure A-2(a). The distance between neighboring planes such as A and B is a/3⟨111⟩. Any of the planes A, B, and C can be transformed to any other plane A, B, or C by a single translation, i.e., they are isomorphic. Thus, if an A plane is translated

(a)
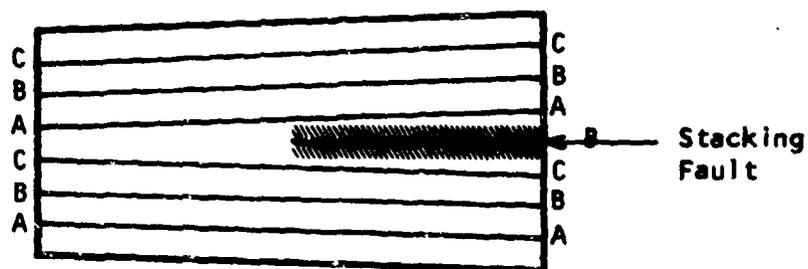
(b)

Extrinsic Stacking Fault
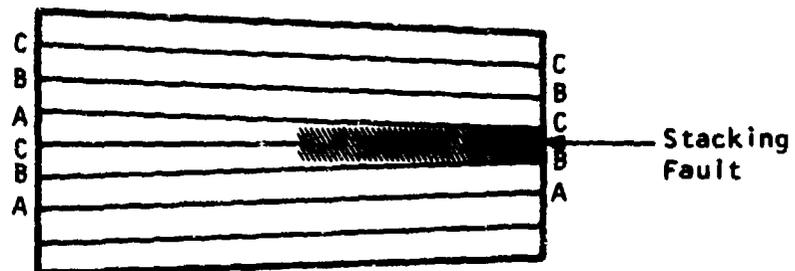
(c)

Intrinsic Stacking Fault

Figure A-2 Stacking Faults in FCC Crystal

through a distance of $a/3\langle 111\rangle$ to the position of a B plane, it would still remain an A plane; but if it were translated by an additional amount, $a/6\langle 11\bar{2}\rangle$, it would be converted to a B plane. Similarly, a B plane can be converted to a C plane by an extra translation of $a/6\langle 1\bar{2}1\rangle$ and a C plane to an A plane by an extra translation of $a/6\langle\bar{2}11\rangle$.

If the normal stacking sequence ABCABC . . . is altered to, for example, ABAB . . . (the stacking sequence for hexagonal symmetry), the resulting defect is called a stacking fault. For example, suppose an extra B plane were inserted between an A and a C plane [Figure A-2(b)]. In this figure the stacking fault is on the right side of the crystal. Note the hexagonal sequences BAB and BCB. Where the stacking fault ends in the crystal there is a partial dislocation. In Figures A-2(b) and (c), these are called Frank partial dislocations and have Burgers vectors of $a/3\langle 111\rangle$. With an extra added plane, the stacking fault is called an extrinsic stacking fault. If, however, a plane of atoms were removed, such as an A plane in Figure A-2(c), an intrinsic stacking fault would be created [again on the right side of Figure A-2(c)]. Again, note the hexagonal stacking sequence BCB in this figure.

Because a (111) plane of one type can be converted to a (111) plane of another type by a translation of $a/6\langle 112\rangle$, an additional type of partial dislocation is possible. This may be accomplished by cutting in a crystal on a (111) plane between an A and a B plane, for example, and translating the bottom of the crystal by $a/6\langle 211\rangle$ before rejoining the crystal across the cut. The result is a Shockley partial dislocation, which has a Burgers vector of $a/6\langle\bar{2}11\rangle$ (Figure A-3). In this figure note the stacking sequence BCB, indicating that the resulting stacking fault is intrinsic in nature [compare with Figure A-2(c)].
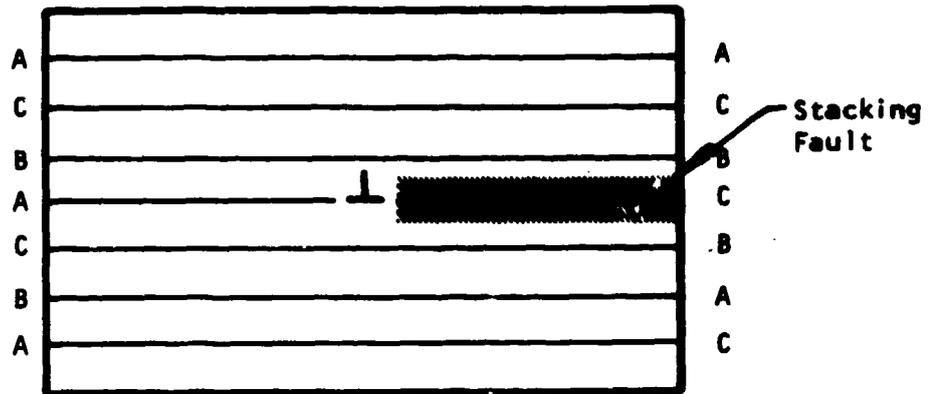
Figure A-3   Shockley Partial Dislocation

Since a partial dislocation is attached to a stacking fault, as the partial dislocation moves, it must create or destroy stacking faults. Thus, a partial dislocation can move only on the plane of a stacking fault to which it is attached. A Frank partial can therefore move only by climb and a Shockley partial only by glide.

APPENDIX B

CCD IMAGER OPERATION

It is appropriate to review the operation of the CCD to clarify the meaning of the data reported in this work. The basic unit of the CCD imager is the MOS capacitor. Imagine a pair of these arranged so that the conducting gate electrodes (ϕ_1, ϕ_2) overlap, as in Figure B-1(a) The p-type substrate is doped with n-type pockets at the edge of each electrode, with the last element a contacted n^+ layer. The output gate OG serves to isolate the n and n^+ regions. The gates ϕ_1, ϕ_2, OG, and the contact to n^+ are electrically insulated from each other.

When none of the electrodes are connected to external voltages, the electrons are in thermal equilibrium throughout the substrate. In normal operation, the substrate is connected to ground; ϕ_1, ϕ_2, and OG are connected to independently controlled power supplies; and the n^+ contact is held at a high positive voltage. Next, the output gate is pulsed positively, lowering the energy of any electrons in the substrate near the oxide interface. By a proper choice of the pulse height, the electrons in the n-pocket under ϕ_2 are "connected" to the n^+ doping region, where they see lower energy states and thus flow to the n^+ where they are collected and swept out by the n^+ power supply. When the pulse under the output gate is removed, the n-pocket under ϕ_2 is depleted. A local charge from the ions remains, and thermal equilibrium is destroyed. Now ϕ_2 is pulsed, lowering the electron energy under all of ϕ_2. This allows the electrons in the n-pocket under ϕ_1 to see the lower (electrostatic) energy levels under ϕ_2 and, as a result, transfer to the n-pocket under ϕ_2. A second pulse on the OG transfers these electrons to the n^+ region and out through the power supply. In practice, it takes several clocking cycles to reach a steady state condition for the time averaged current through the n^+ supply. Once this condition is reached, the electron energy for zero volts on ϕ_1, ϕ_2, and OG is as shown in Figure B-1(b). Also
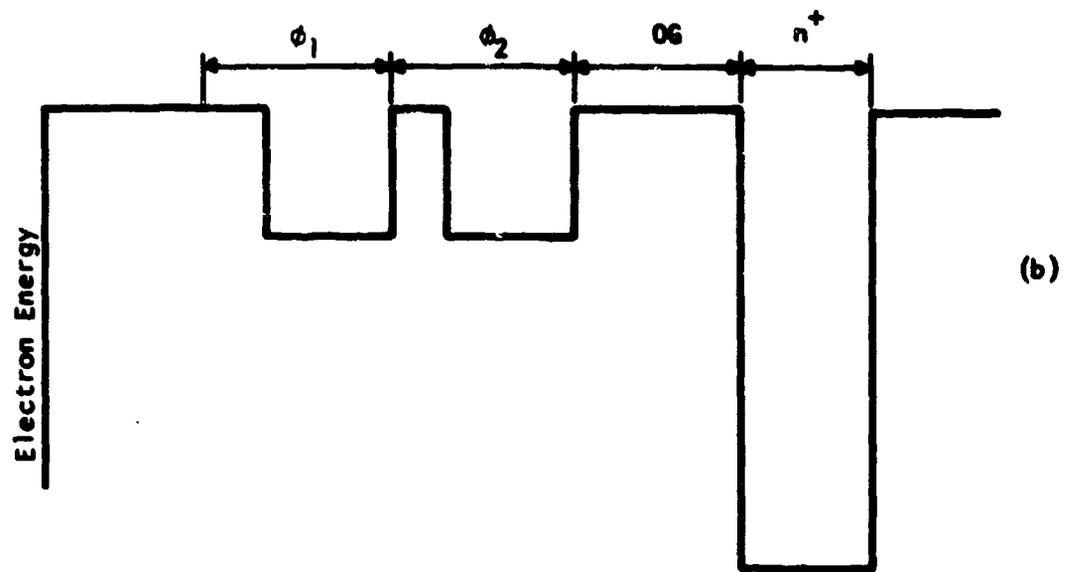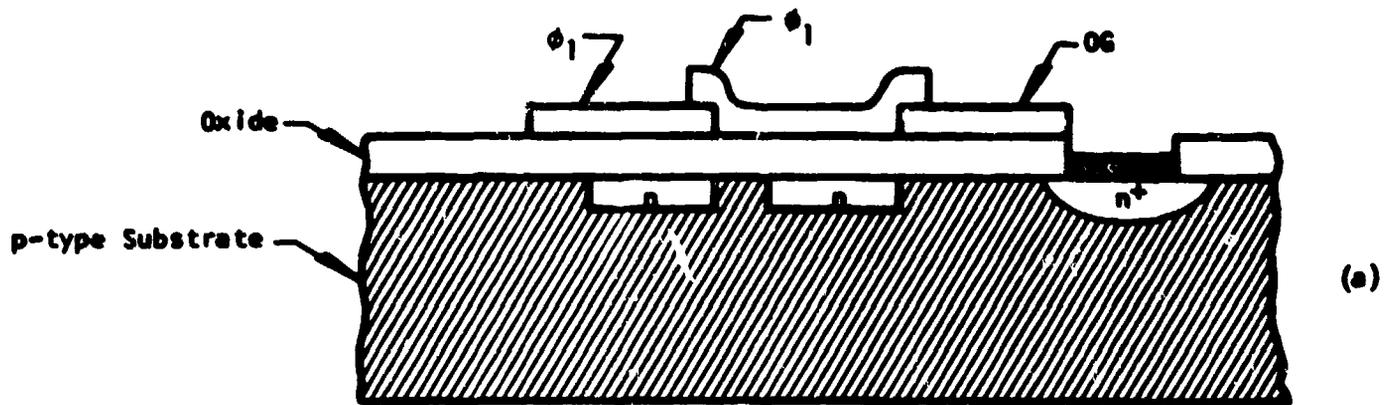
Figure B-1 Minimum Device Structure of the Two-Phase CCD. (a) Circuit architecture, (b) electron energy profile at depletion.

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shown are the regions controlled by each of the four power supplies. Note that the fraction of the region under ϕ_1, ϕ_2 which is not n-doped serves as a barrier to isolate the n-pockets.

In the steady state, the current through the n^+ supply is called the "dark current" since it is measured in the dark where only thermal carrier generation can occur.

If the ϕ_1, ϕ_2 structures are repeated to the left in Figure B-1(a), a serial register is generated. In this case, the first pulsing of the ϕ_2 gates, which are bussed together, will merge the charge under the ϕ_1 gates with that already present under ϕ_2. This merged charge is the unit propagated to the n^+ contact. The minimum spatial resolution element therefore corresponds to the combined area of ϕ_1 and ϕ_2 and is called a "pixel," for picture element.

Each electron pulse is fed to a video monitor where the intensity of the display is arranged to be proportional to the number of electrons in the pixel. In the ideal case there would be no contrast on this display because the thermal generation rate would be the same in each pixel. If, however, an electrically active defect occurred in one pixel, then the resulting white spot on the video display (dark current spike) will reveal both its occurrence and location on the device. In practice, the sensitivity to defects is enhanced by allowing the device to integrate charge (ϕ_1, ϕ_2 at dc) for a small time (we use 30 ms) between video readouts. The integration time must be short compared to the time necessary for the majority of pixels to return to thermal equilibrium, but long enough to reveal the electrically active defects with good video contrast.

When the generation rate in a given pixel is exceptionally high, every video pulse will be high in intensity, corresponding to a fully loaded

n-pocket, because every pixel read into the n^+ region necessarily goes through the defective area. The video display for this case consists of a white line. Certain processing errors, however, also cause white lines. In any event, we have chosen to ignore these white lines in the discussion of this work because their presence does not represent, in principle at least, a new type of phenomenon to be investigated.

The imager used in this work is particularly well suited to the study of electrically active defects because the ratio of pixel area to total device area is high, 0.74. On a three-inch slice, some area near the edge is lost to partial, nonoperating devices. Even so, 51% of the total slice area has accessible pixels whose size [25.4 μm x 25.4 μm (1 mil x 1 mil)], makes it easy to locate defective areas for subsequent structural analysis.

APPENDIX C
CCD IMAGER FABRICATION

The CCD imagers used to image the dark current patterns and point defects investigated under this contract are two-phase, n-channel, buried channel imagers with 82 K resolution elements in a 0.55 cm^2 active imaging area. Each element's area is 671 μm^2 ($\sim$ 1 mil^2). The structure is a serial-parallel-serial, full-frame format with polysilicon and aluminum electrodes. The imager stores the matrix of charge packets in the imaging area and transfers the packets, one line at a time, into the output serial register, where each element is sensed at a 6.44 MHz sample rate.

The imagers are fabricated on 7.6 cm (3 inch) diameter p-type (100) 8 to 12 Ω-cm silicon slices.

The basic process flow, shown in Figure C-1, is summarized below:

(1) After an initial cleanup of the slices, an initial oxide is grown. A CVD nitride etch and diffusion mask is deposited on the initial oxide.

(2) The moat region is patterned, using optical photolithographic techniques, and the nitride is etched. Using the nitride as an etch mask, the initial oxide is etched. A subsequent boron diffusion dopes the p regions of the device.

(3) A long oxidation cycle grows a thick field oxide in the moat and channel stop regions of the imager.

(4) Regions to receive n^+ doping, such as source/drain regions, are then opened by nitride and oxide removal. A phosphorus diffusion forms the n^+ regions.

(5) At this point, the initial thin oxide is stripped back to the silicon, and an oxidation is performed to achieve a clean, high integrity, gate oxide.

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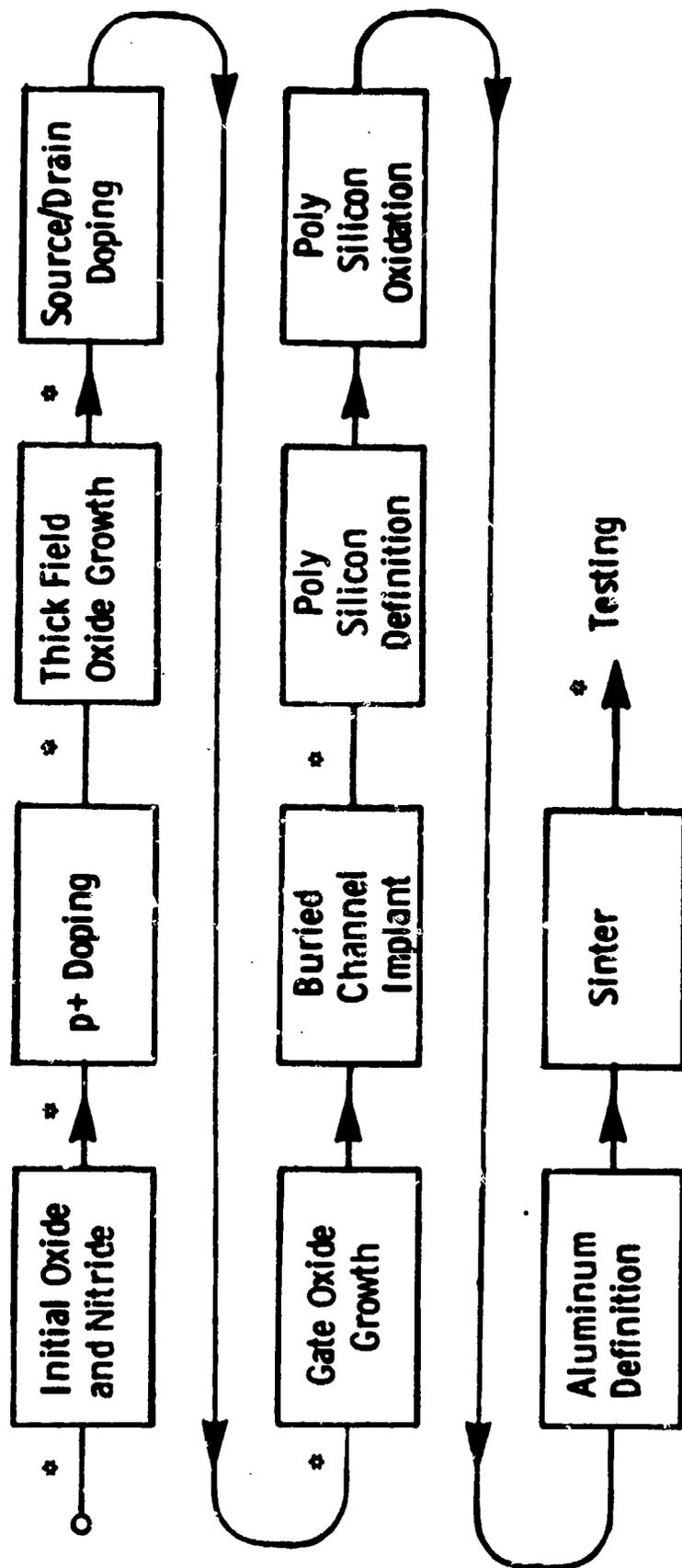
Figure C-1 CCD Imager Process Flow Diagram

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(6) The buried channel doping is then implanted through the gate oxide, and a second oxidation is performed to grow the gate to its final thickness.

(7) CVD polysilicon deposition and patterning and dopant implants to form the barriers and wells are performed to accomplish a self-aligned phase electrode with the barriers and wells. The barriers and wells provide the directionality required for a 2ϕ device.

(8) A thermal oxidation of the polysilicon forms the interlevel insulation required to isolate the phase-one (polysilicon) electrode from the phase-two (aluminum) electrode to be patterned.

(9) After the oxide has been removed from the contact regions, aluminum is deposited on the slice. The aluminum electrode and lead pattern is masked and etched.

(10) The aluminum-to-silicon contacts are sintered to reduce the contact resistance. The devices have then completed fabrication.

During the fabrication cycle, the highest temperature encountered is 1100°C. All high temperature operations are performed with a slow push and slow pull to prevent thermal shock in the slices.

Figure C-2 shows a cross-sectional view of the phase electrodes and the implants that form the wells.

Thick field channel stops with excess p-type doping separate the CCD channels. These stops are formed during step (3) above.

The device is doped so that the depletion region from the buried channel extends ~5 μm into the Si from the gate oxide - silicon interface. All electrically active defects that reside in this depletion region will generate dark current signal. Defects outside the depletion region can contribute only after the carriers diffuse to the CCD wells.

Device testing is described in Appendix B of this report.
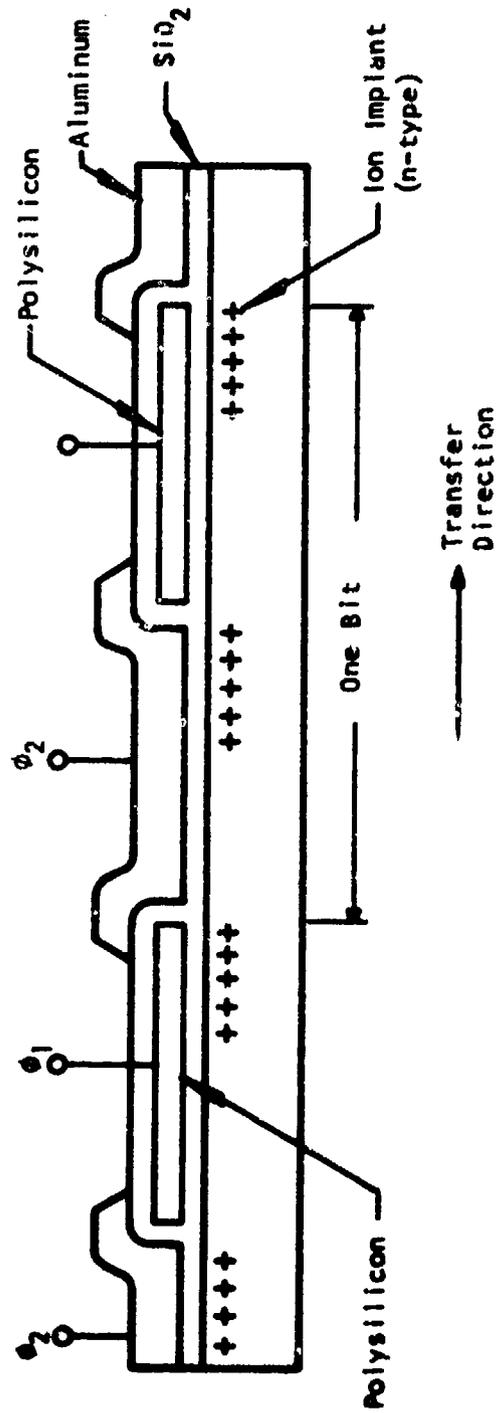
Figure C-2 Device Cross Section Showing Profile Along Transfer Direction

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APPENDIX D

X-RAY TOPOGRAPHY

The arrangement for transmission x-ray topography is illustrated in
Figure D-1. In this figure we are looking down on the apparatus. The slits
closest to the x-ray source limit the horizontal divergence of the x-ray beam
so that only the $K\alpha_1$ component is diffracted by the sample. The second set of
slits prevents the main beam from falling on the film, allowing only the
diffracted beam to expose the film. Since the first set of slits defines a
line of x-rays normal to the figure, the film and sample are scanned through
this beam to form an image on the film of the diffracted x-ray intensity from
the entire sample. Reflection topography is similar, except that the
diffracted beam emerges from the same side of the sample as the incident beam.
Since the main beam now passes through the sample, the second set of slits is
not needed and is usually omitted.

Conditions that lead to the maximum detectability of defects by x-ray
topography were considered in some detail in the first technical report[36] and
will not be repeated here. It was shown that the practical resolution and
sensitivity of a topograph were x-ray photon noise limited. Therefore, to see
a defect whose area on the topograph is A and whose diffracted intensity is ΔI
above the background intensity I, an exposure E is needed such that

$$\frac{\Delta I}{I}\{E\ A[1\ -\ \exp(-\ \mu_o t)]\}^{\frac{1}{2}}$$

is greater than some number (theoretically 2 for the 95% confidence limit).
The term in square brackets is the fraction of x-ray radiation adsorbed by the
topographic film. The limitation imposed by conventional photographic
processes is that the plates will withstand exposures of the order of 10
photons/μm^2 before developing to a totally black plate. Since the plates are
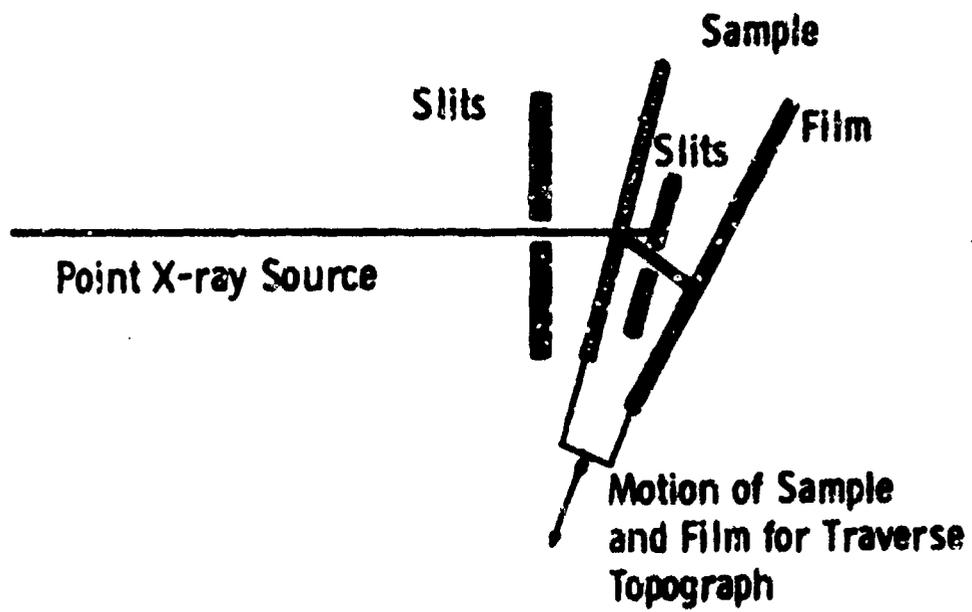
Figure D-1   Transmission X-Ray Topography

capable of recording exposures to the order of 1000 photons/μm^2, we have explored the use of an alternate developer to reveal the latent image.

The use of a fine-grain developer in conjunction with long exposure times was found to significantly reduce the graininess of the developed image, which is due to the statistical fluctuation of the intensity of x-rays, and give significantly higher resolution topographs. The developer used was[37]

    0.45 g Elon developing agent
       3 g Ascorbic acid
       5 g Borax
       1 g Potassium bromide
    Water to make 1 liter.

The developer is unstable and is therefore mixed two hours prior to use and discarded after development is complete. The exposure-density characteristics of this developer at room temperature on 25 μm Ilford L-4 nuclear plates exposed to Cu$K\alpha_1$ radiation is shown in Figure D-2. In making long-exposure topographs, the development time is adjusted to give good plate density (average $\approx$ 2) for the exposure given to the plate.

To understand the position of defects in the imager, it is necessary to understand the contrast from the device itself.

Figure D-3(a) is a 422 reflection topograph of an imager that contains a surface scratch applied after device fabrication. The same scratch is visible in an optical micrograph of the imager in Figure D-3(b). The channels in the optical micrograph can be readily identified since they contain additional surface relief arising from the oxidation of the polysilicon. This relief is not found on the channel stops. The scratch, therefore, is seen to lie entirely on the higher channels.

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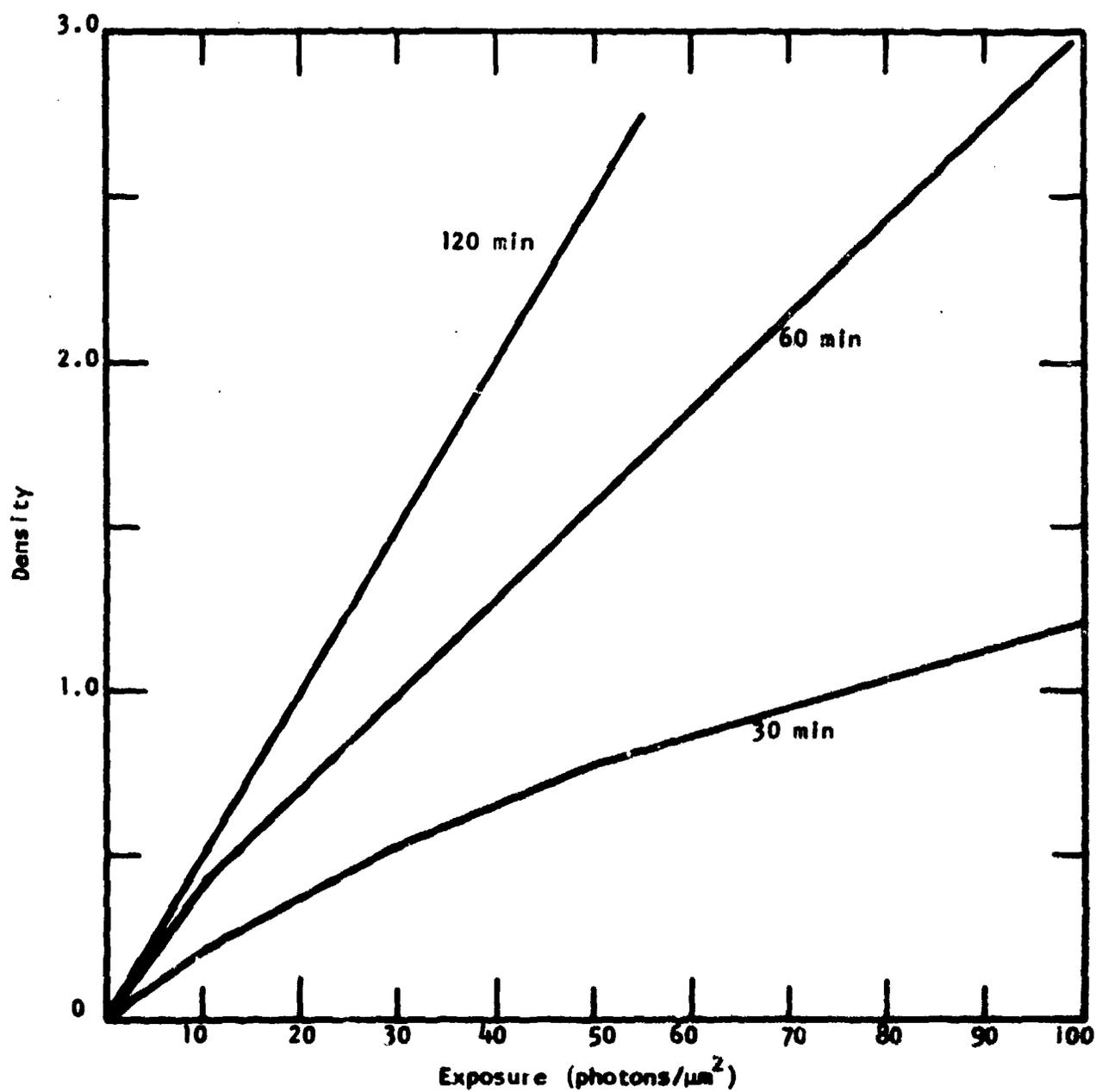
Figure D-2 Density vs Exposure Curves for Elon-Ascorbic Acid Developer at Various Development Times. Ilford L-4 25 μm emulsion, Cu$K\alpha_1$ radiation.

$\vec{g} = 422$

(a)

Channel Stop

Channel

(b)

$\vec{g} = 42\bar{2}$

100 µm

(c)
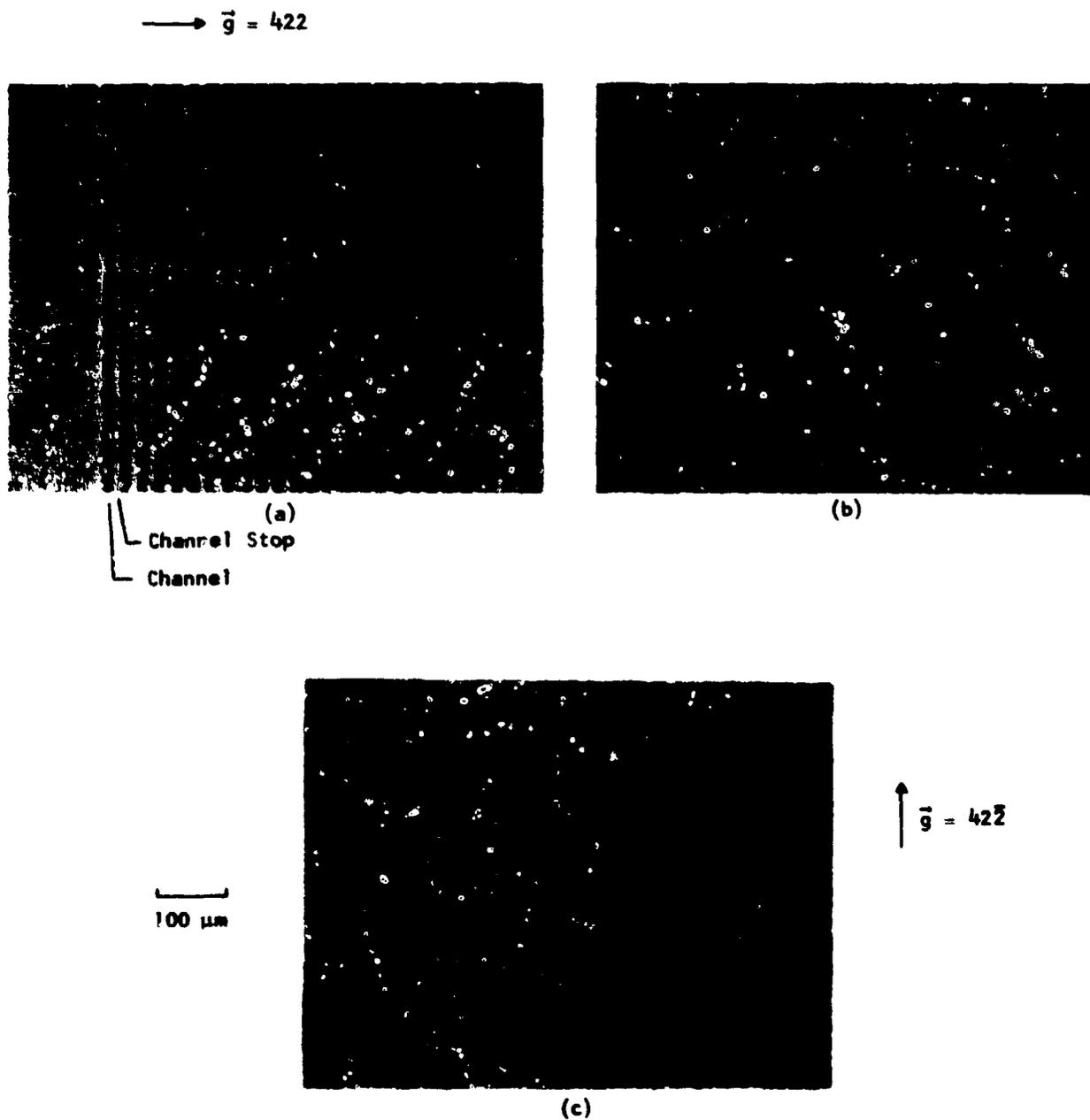
Figure D-3   Postprocessing Scratch in CCD Imager.   (a) 422 reflection topograph. (b) optical photograph, (c) 422 reflection topograph.   (a) and (c) are mirror images of (b).

Figures D-3(a) and D-3(b) show that for the 422 reflection, the channels appear dark in the topograph, while the channel stops appear light. This type of contrast arises from the surface relief of the imager. This may be qualitatively understood by reference to Figure D-4. The channel stop is recessed as a result of the thick oxide growth over the channel stop. The protruding channels therefore intersect a proportionately larger amount of the x-ray beam than do the channel stops, and, subsequently, cast a shadow on the channel stops. Thus, the channels receive a higher incident x-ray intensity than the channel stops, and have, therefore, a higher diffracted intensity for this reflection. The exact diffraction process is somewhat more complicated and requires considerations of energy flow from the dynamical theory to be fully explained. We find, for example, that the diffracted intensity from this reflection is higher than that of the 42$\bar{2}$ reflection [Figure D-3(c)], for which the surface relief of the channels and channel stops plays no part. This shows that there is an additional enhancement in overall diffracted intensity that is not accounted for in the simple argument given above.

The same scratch, imaged in a 42$\bar{2}$ reflection, is shown in Figure D-3(c). The faint black bands running from left to right arise from the same type of contrast mechanism as the bands in Figure D-3(a), but the surface relief is substantially less. The horizontal dark band corresponds to the silicon under the polysilicon gate, while the light band is under the aluminum gate. This surface relief results from the process step where the polysilicon is oxidized, causing additional oxidation of the silicon substrate that is not covered by the polysilicon. The channels and channel stops, which are very faint, may be seen by viewing the image at a glancing angle from the bottom of the page. By correlating Figures D-3(b) and D-3(c), it will be seen that the channels appear light, while the channel stops are darker. This contrast arises from the strain field of the doping in the channel stop.

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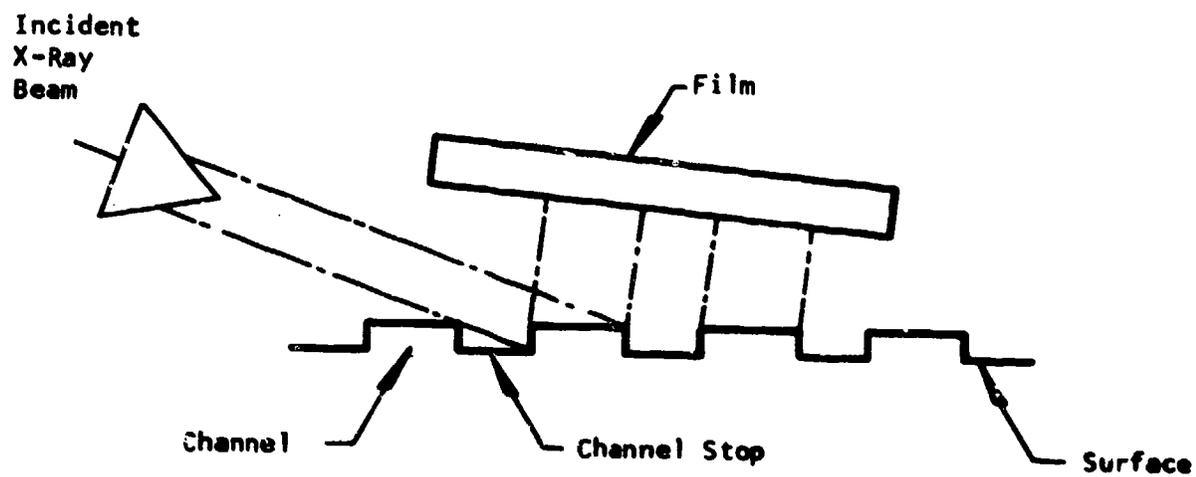
Figure D-4 Experimental Arrangement for 422 Topograph Illustrating Surface
Relief Contrast Mechanism

Figure D-5 is a topograph of such a defect which was found in a nonoperational portion of a device on float-zoned material. Defects labeled "1" are dislocations emergent from the bulk of the material, as confirmed by transmission topography. Defect "2" is a dislocation that has grown off an emergent dislocation from the bulk, labeled "3."

A reflection topograph of this same region under a different diffraction condition is shown in Figure D-5(b). Several important points are illustrated in these topographs. First, close examination of Figures D-5(a) and D-5(b) shows all defect images are split. This double contrast arises from the strain field of a single dislocation with an edge component. According to the kinematical theory of image formation[38,39] lattice planes that are tilted more than ~ 2 times the angle over which the perfect crystal diffracts will diffract kinematically, giving an added intensity. For a dislocation with an edge component, there are two such regions, one on either side of the core (Figure D-6), and hence the bimodal contrast pattern. Such a splitting has previously been observed in transmission topographs, where the diffraction conditions used caused the splitting to be ~ 5 times that in our topographs.[39] The observed total image size is in the range of what is theoretically expected for a single dislocation. According to Lang and Polcarova,[40] the image width of a dislocation is given by

$$W = C \frac{\vec{g} \cdot \vec{b}}{2\pi} \xi_g \quad .$$

where C is a constant somewhat greater than unity, and ξ_g is the extinction distance of the x-rays for the reflection under consideration. The extinction distance depends on the angles that the incident and diffracted x-ray beams make with the surface. In our case, the incident radiation can enter the crystal at either a glancing angle on the channel and channel stop top surfaces, or nearly perpendicular to the crystal at the edge separating the channel and channel stop; hence, we have a situation more complex than that

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$\vec{g} = 422$

(a)

100 um
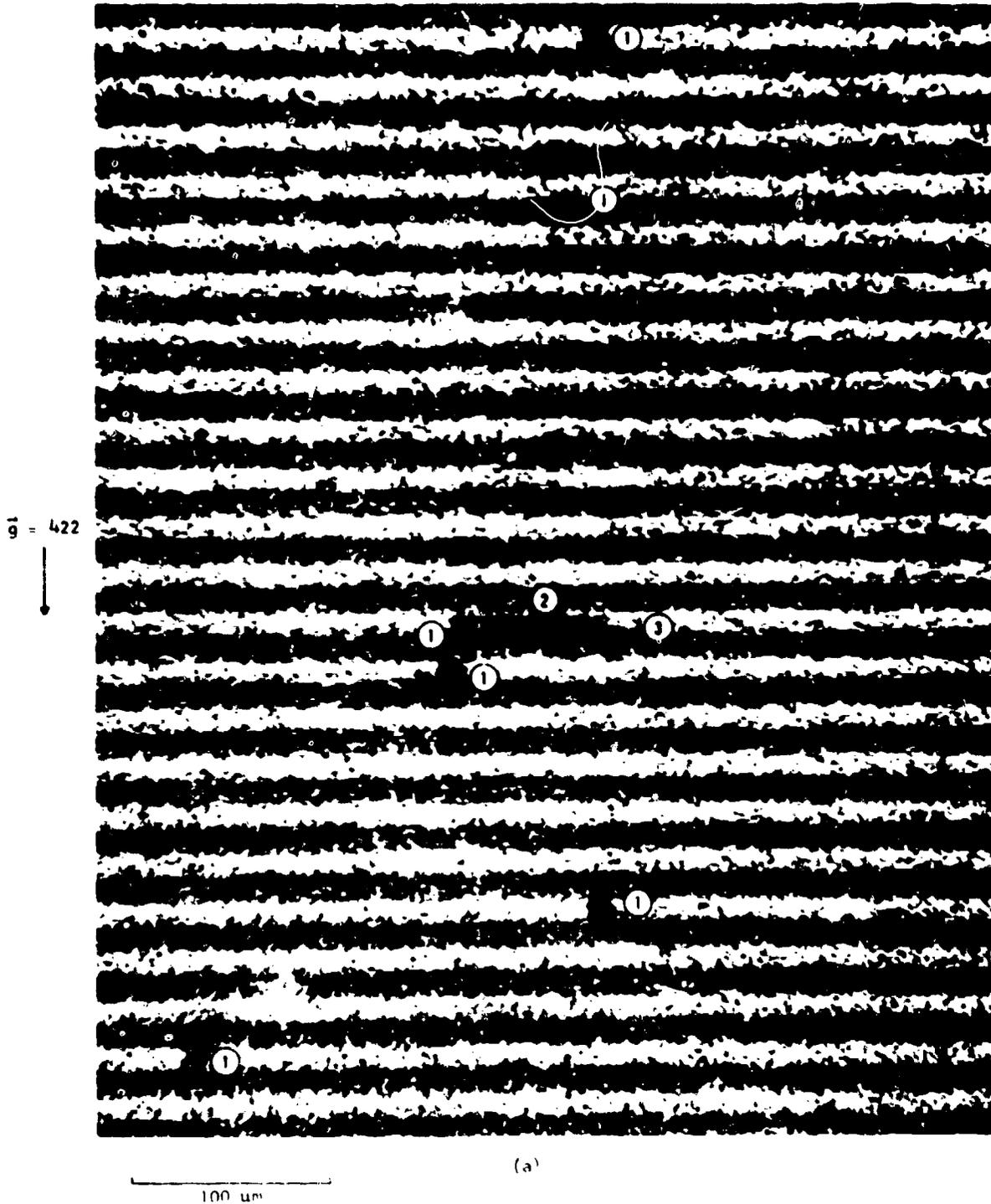
Figure D-5   Topograph of Dislocations in Device on Float-Zoned Material

$\vec{g} = 4\bar{2}\bar{2}$
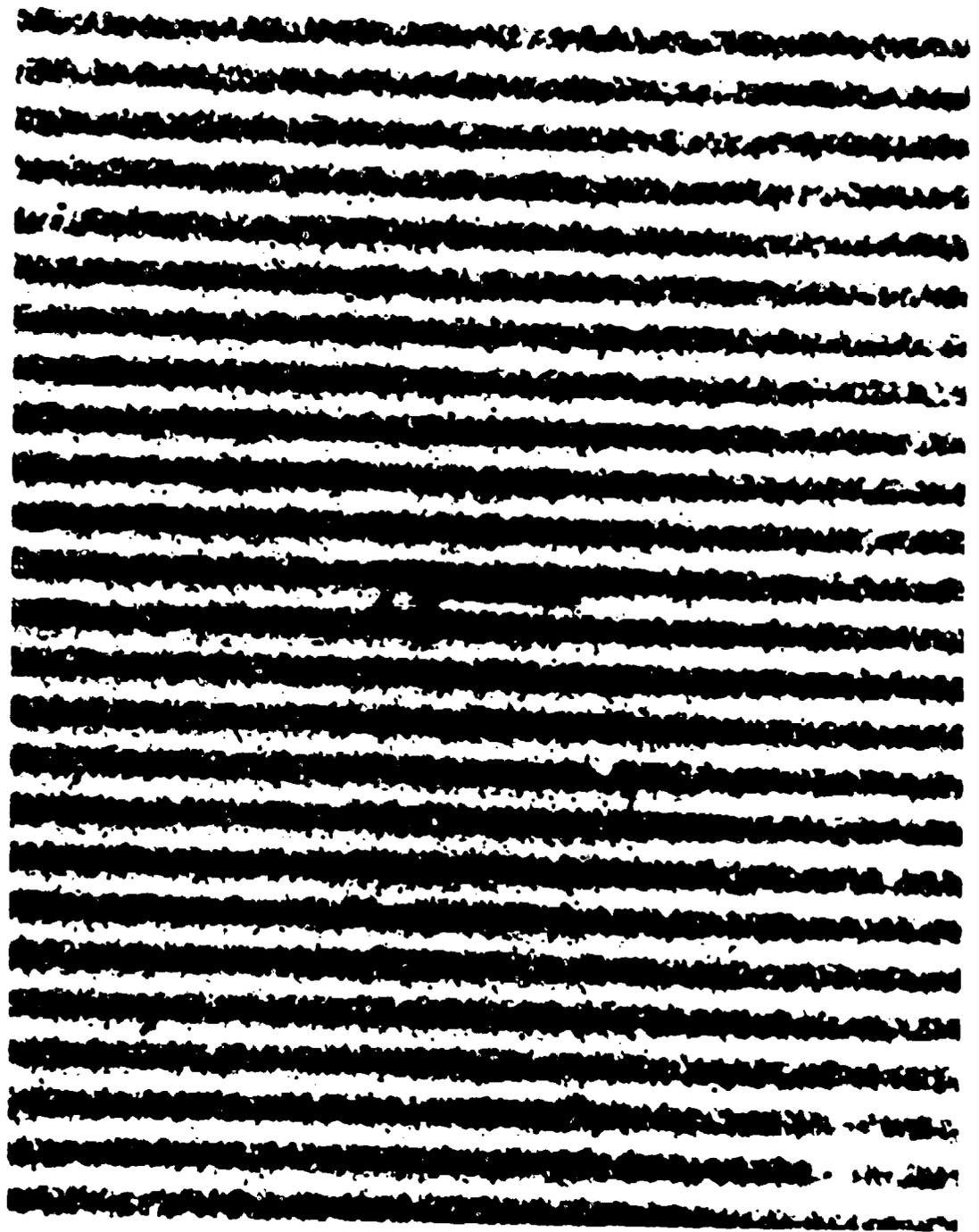
100 um   Figure D-5   (Continued)
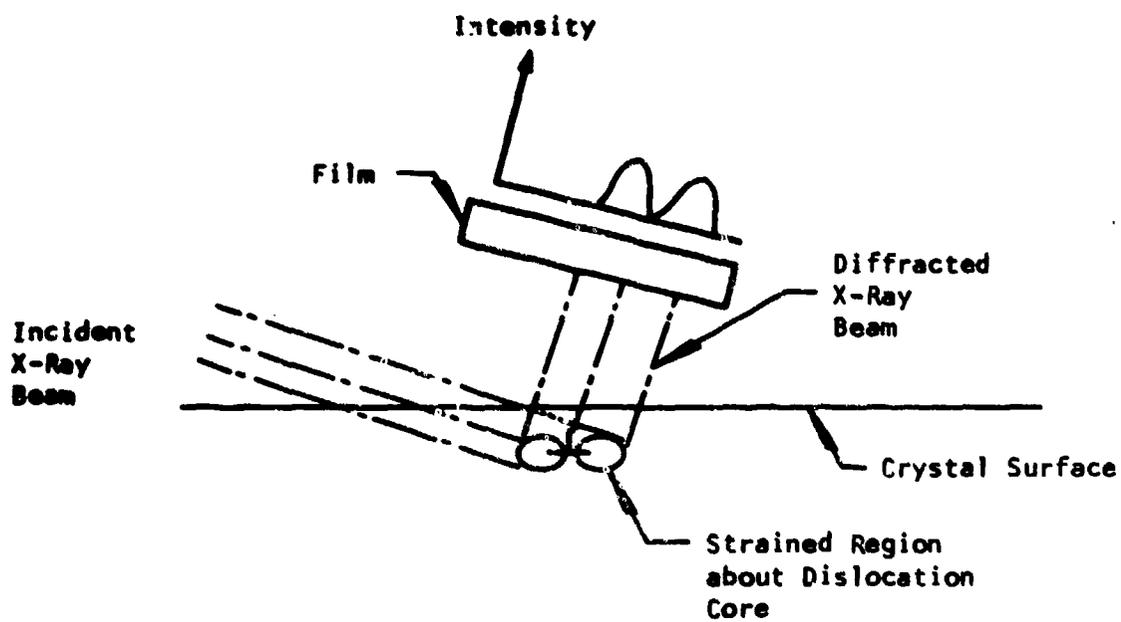
Figure D-6   Origin of Bimodal Contrast from an Edge Dislocation

derived for the simple theory. If we assume, however, that the x-ray field in the crystal arises entirely from the glancing incidence radiation, then ξ_g is calculated to be 8.3 μm, meaning the width is given by

$$W = 1.32 \ C \ \vec{g} \cdot \vec{b} \ \mu m \quad .$$

Now if $\vec{g} \cdot \vec{b} = 3$ [which is the case for $\vec{b} = \frac{1}{2}(101)$], and if $C \approx 2$, then the calculated and observed image size would agree. The effect of the radiation incident on the channel/channel stop edge should be to increase the extinction distance, allowing for a smaller value of C for agreement.

Comparison of Figures D-5(a) and D-5(b) also shows that the image of the channels and channel stops is shifted from the image of the defects in these topographs. A study of several pairs of topographs indicates that this shift is approximately 5 μm between the two topographs for the (224) type of reflections. This means that in each of the two topographs, which are symmetrically related by a 180° rotation of the device, the image of the channels and channel stops is shifted 2.5 μm toward the incident x-ray beam (in the direction of the $\vec{g}$ vector), and hence the correct location of the defect is in a position 2.5 μm in the direction of the $\vec{g}$ vector.

APPENDIX E
TRANSMISSION ELECTRON MICROSCOPY

The transmission electron microscopes used in these investigations were a Siemens IA operating at 125 kV and a JEOL100CX operating at 100 kV. The latter instrument is equipped with a field emission gun, a STEM attachment, and energy dispersive x-ray analyzer. The techniques used to reach the conclusions presented are standard and are well treated in the books by Loretto and Smallman,[41] and by Hirsch, et al.[42] The weak beam technique is dealt with in papers of Ray and Cockagne.[43,44]

The sample preparation technique is summarized below.

(1) The specimen was ground to a thickness of ~ 100 μm.

(2) The specimen was chemically thinned to a thickness ~ 25 μm.

(3) A stainless steel ring, 3 mm diameter, was then attached over the desired specimen area using a mixture of photoresist and carbon paint. Paraffin was placed in the center of the ring, and the specimen disk etched out.

(4) After removal of the paraffin, the sample was mounted on paraffin, and the sample thinned to the desired thickness of ~ 1 μm.

The etchant used was that originally reported by Lawrence,[45] with the HF concentration adjusted to give the desired etch rate.

With this procedure, it was found possible to consistently obtain areas sufficiently thin for electron transmission of 250 μm x 250 μm in the desired area of a device.

REFERENCES

1. G. H. Schwuttke, K. Yang, and H. Kappert, Phys. Status Solidi A 42, 553 (1977).

2. T. Y. Tan and W. K. Tice, Philos. Mag. 30, 615 (1976).

3. T. Y. Tan, E. E. Gardner, and W. K. Tice, Appl. Phys. Lett 30, 175 (1977).

4. G. H. Schwuttke and K. H. Yang, Technical Report No. 2 for Contract No. N00173-76-C-0303, September 1977.

5. D. M. Maher, A. Staudinger, and J. R. Patel, J. Appl. Phys. 47, 3813 (1976).

6. J. R. Patel, K. A. Jackson, and H. Reiss, J. Appl. Phys. 48, 5279 (1977).

7. S. Yasuami, M. Ogino, and S. Takasu, J. Cryst. Growth 39, 227 (1977).

8. J. T. Yue and H. Ruiz, in Semiconductor Silicon 1977, H. R. Huff and E. Sirth, eds. (Electrochemical Society, New York, 1977), p. 596.

9. I. R. Sanders and P. S. Dobson, Philos. Mag. 20, 881 (1969).

10. I. L. F. Ray and D. J. H. Cockayne, Proc. R. Soc. A 325, 543 (1970).

11. A. Gomez, D. J. H. Cockayne, P. B. Hirsch, and V. Vitek, Philos. Mag. 30, 105 (1975).

12. H. Foll and B. O. Kolbesen, in Semiconductor Silicon 1977, loc. cit., p. 740.

13. G. R. Booker, Discuss. Faraday Soc. 38, 298 (1964).

14. K. V. Ravi and C. J. Varker, J. Appl. Phys. 45, 263 (1974).

15. R. Ogden and J. M. Wilkinson, J. Appl. Phys. 48, 412 (1977).

16. H. Hashimoto, H. Shibayama, H. Masaki, and H. Ishikawa, J. Electrochem. Soc. 123, 1899 (1976).

17. K. V. Ravi, Philos. Mag. 30, 1081 (1974).

18. C. J. Humphreys, A. Howie, and G. R. Booker, Philos. Mag. 15, 507 (1967).

19. K. V. Ravi, C. J. Varker, and C. E. Volk, J. Electrochem. Soc. 120, 533 (1973).

20. Y. Takano and M. Maki, in Semiconductor Silicon 1973, H. R. Huff and R. R. Burgess, eds. (Electrochemical Society, New York, 1973), p. 469.

21. D. Bialas and J. Hesse, J. Mater. Sci. 4, 779 (1969).

22. J. B. Warren and J. J. Hren, Thirty-Fourth Annual EMSA Meeting, 1976, p. 488.

23. C. L. Claeys, E. E. Laes, G. J. Declerck, and J. Van Overstraeten, in Semiconductor Silicon 1977, loc. cit., p. 773.

24. K. Tanikawa, Y. Ito, and H. Sei, Appl. Phys. Lett. 28, 948 (1976).

REFERENCES
(continued)

25. A. J. R. deKock, in Semiconductor Silicon 1977, loc. cit., p. 508.

26. K. Graff, J. Hilgarth, and H. Neubrand, in Semiconductor Silicon 1977, loc. cit., p. 575.

27. P. E. Freeland, K. A. Jackson, C. W. Lowe, and J. R. Patel, Appl. Phys. Lett. 30, 31 (1977).

28. A. F. Tasch, Jr., D. D. Buss, H. R. Huff, C. E. Hartmann, and V. R. Porter, in Semiconductor Silicon 1973, loc. cit., p. 658.

29. S. M. Hu, Appl. Phys. Lett. 31, 139 (1977).

30. S. Kawado, Y. Hayafuji, and T. Adacki, 1975 Fall Meeting of the Electrochemical Society, Extended Abstracts Volume 75-2 (Electrochemical Society, New York, 1975), p. 477.

31. J. P. Hirth and J. Lothe, Theory of Dislocations (McGraw-Hill, New York, 1968), pp. 353-362.

32. K. Wessel and H. Alexander, Philos. Mag. 35, 1523 (1977).

33. G. A. Rozgonyi, P. M. Petroff, and M. H. Read, J. Electrochem. Soc. 122, 1725 (1975).

34. J. P. Hirth and J. Lothe, Theory of Dislocations (McGraw-Hill, New York, 1968).

35. F. R. N. Nabarro, Theory of Crystal Dislocations (Oxford Press, London, 1967).

36. H. F. Schaake and W. C. Rhines, Texas Instruments Incorporated, "Characterization of Electrically Active Defects in Si Using CCD Image Sensors," Quarterly Technical Report No. 1 for Contract No. N00173-76-C-0281, October 1976.

37. J. F. Hamilton and L. E. Brady, J. Appl. Phys. 30, 1495 (1953).

38. B. K. Tanner, X-Ray Diffraction Topography (Pergamon Press, Oxford, 1976).

39. A. Authier, Adv. X-Ray Analysis 10, 9 (1967).

40. A. R. Lang and M. Polcarova, Proc. R. Soc. A 285, 297 (1965).

41. M. H. Loretto and R. E. Smallman, Defect Analysis in Electron Microscopy (Chapman and Hall, London, 1975).

42. P. B. Hirsch, A. Howie, R. B. Nicholson, D. W. Pashley, and M. J. Whelan Electron Microscopy of Thin Crystals (Butterworths, Washington, 1965).

43. D. J. H. Cockayne, I. L. F. Ray, and M. J. Whelan, Philos. Mag. 20, 1265 (1969).

REFERENCES
(continued)

44. D. J. H. Cockayne, I. L. F. Rav, and M. J. Whelan, Proceedings of the Seventh International Conference on Electron Microscopy $\underline{2}$, 277 (1970).

45. J. E. Lawrence and H. Koehler, J. Sci. Instrum. $\underline{42}$, 270 (1965).